IWES 2017

2nd Italian Workshop on Embedded Systems

Rome – 7-8 September 2017

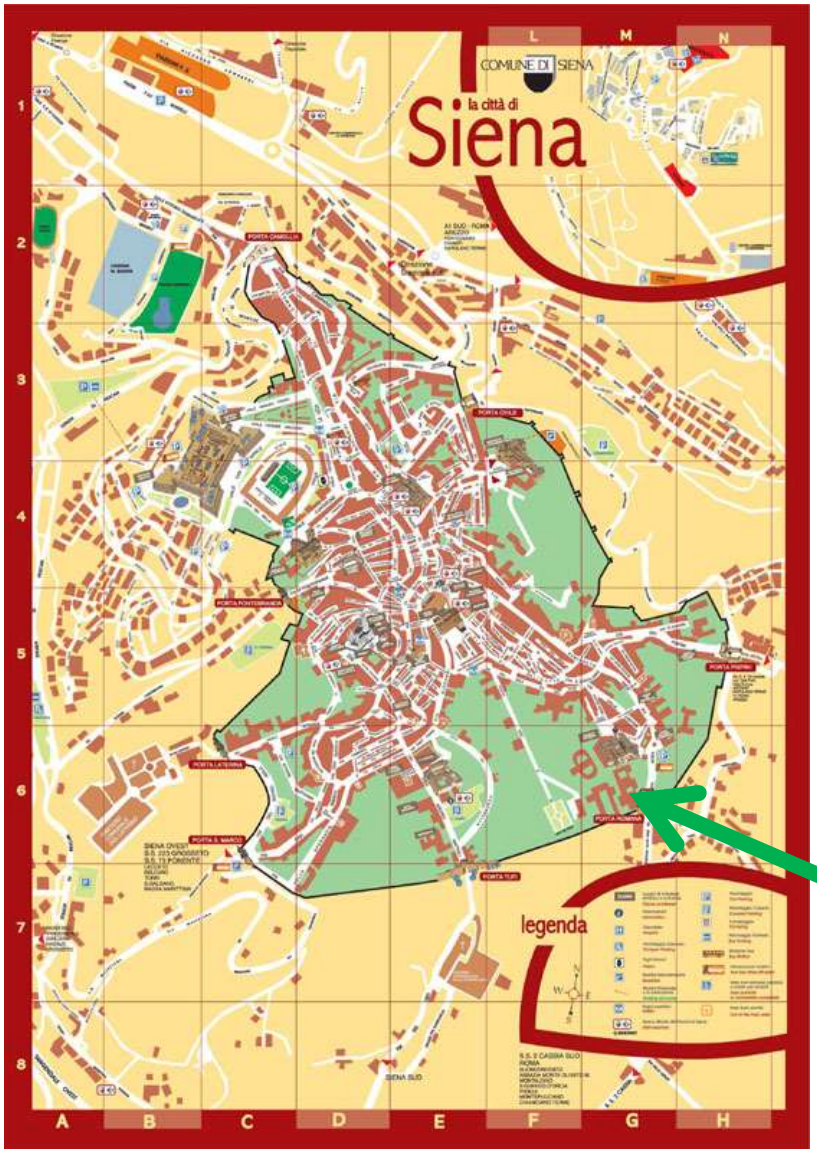
UNISI Research Group Overview

Roberto Giorgi
University of Siena, Italy

http://www.dii.unisi.it/~giorgi


Milano
Bergamo
Verona
Venezia
Treviso
Trieste
Padova
Pavia
Torino
Asti
Parma
Modena
Bologna
Ravenna
Genova
Savona
La Spezia
Cesena
Rimini
San Marino
Pisa
Firenze
Livorno
Nizza
Arezzo
Siena
Ancona
Italia
San Benedetto del Tronto
Grosseto
Ascoli Piceno
Terni
Pescara
Chieti
Vasto
Bastia
Parc Naturel Régional de Corse
Corsica
Ajaccio
Porto Vecchio
Roma
Fiumicino
Frosinone
Latina
Foggia
Andria
Napoli
Pompei
Salerno
Potenza
Stintino
Olbia
Sassari
Alghero
Parenzo
Rovigno
Pola
Fiume
Croazia
Zara
Sibenico
Spalat
Mare Adriatico
E70
E45
E612
E35
E717
E76
E65
E71
E842

Engineering Faculty in Siena



~2km

Our venue

Computer Architecture Lab

Research Group @ UNISI

- 1 Associate prof.: Roberto Giorgi + 1 Aggregate prof.: Sandro Bartolini
- Cooperation with prof. Antonio Rizzo
  - 1 PhD Student, 1 Kernel Hacker, 1 Grant research student
  - HR Throughput: 2 Full-Prof., 2 Researchers, 9 Postdocs, 7 PhD students -- -- during the last 7 years
- Courses by me:
  - Bachelor (L1): **Computer Architecture** (6 credits) -3rd year (Italian)
  - Master (L2): **High Performance Computer Architecture** (9 credits) – 1st and 2nd year(English)
- Lab Resources
  - 64-core (x86) CC-NUMA w/1024GiB RAM
  - 48-core+256GiB, about 15 simulation servers (8-core+32GiB)
  - 12 different FPGA boards ranging from Virtex-6 to Zynq Ultrascale+ (6-core 64 bits)
  - Xeon Phi, Maxeler Dataflow computer, GPUs, 50+ embedded boards, (20+ workstations)

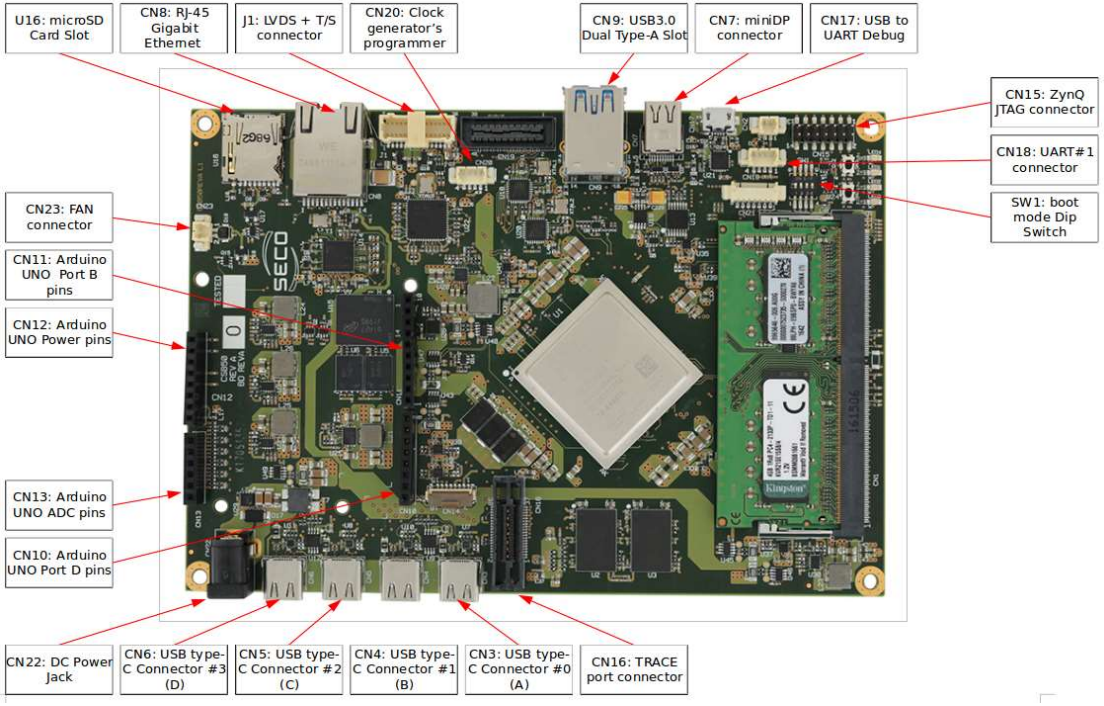
Cooperation with Laboratorio Nazionale Embedded Systems and Smart Manufacturing (LN-ESSM) CINI

- CINI lab LN-ESSM (in progress) director prof. Antonino Mazzeo
- UNISI competences
  - (Giorgi, Bartolini) Programmable Hardware, Processors, Co-processors and Microcontrollers
  - (Giorgi) Hardware/software projects ecosystems
  - (Giorgi) Smart Cyber-Physical Systems architectures
  - (Giorgi, Rizzo) Smart Systems Integration and Internet of Things Applications
  - (Rizzo) Human Machine Interface
  - (Bartolini) Efficient programmability of heterogeneous multi-/many-core systems with single source code
  - (Bartolini) Hardware and software for security and trust
  - (Bartolini) Energy Management, power efficiency and approximate computing in embedded nodes

AXIOM

Agile, eXtensible, fast I/O Module for the cyber-physical era

2015-2017 -- 4Meuro funding
Coordinator: Roberto Giorgi



University of Siena
(Coordinator Partner)

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

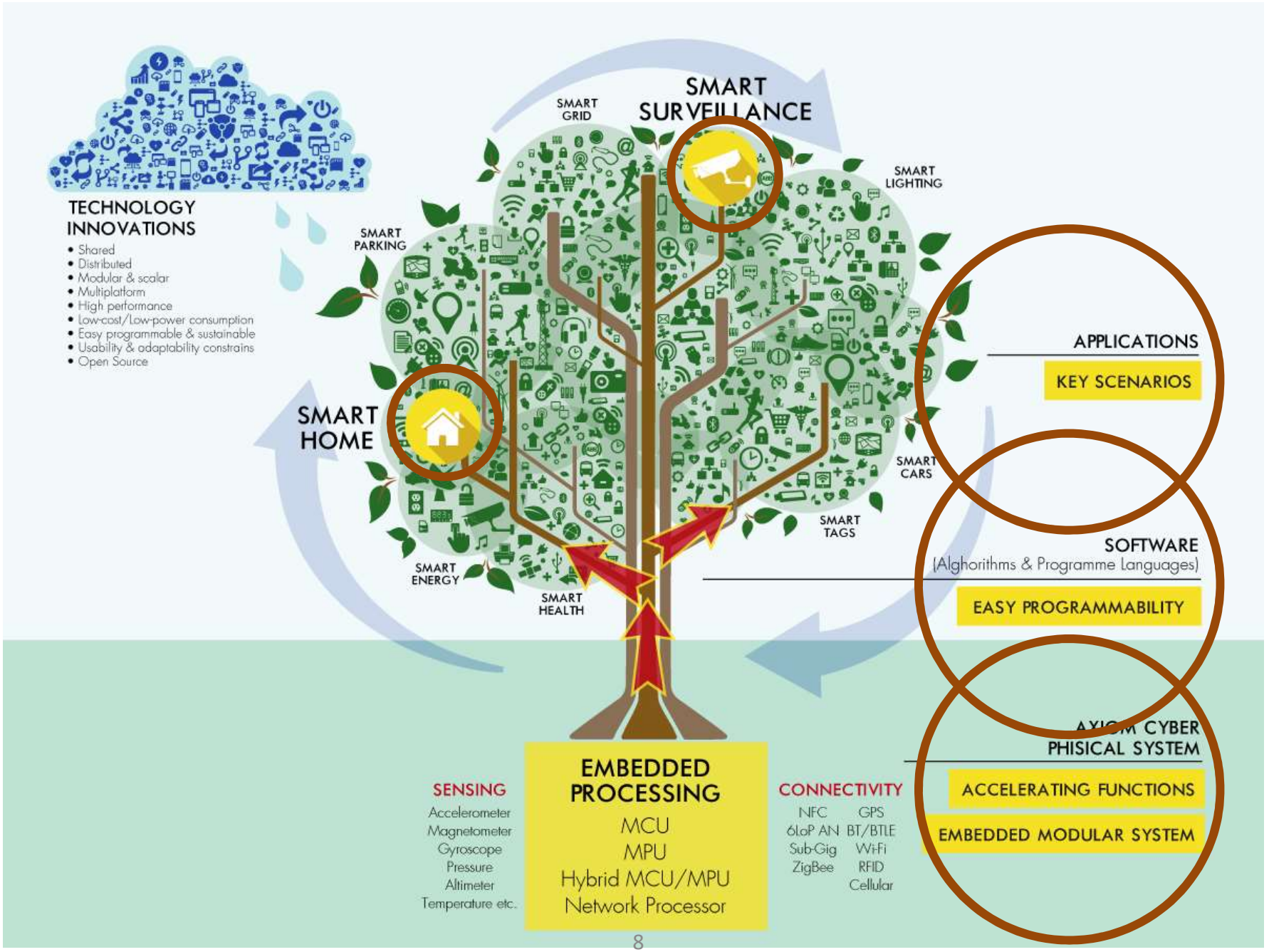
EVIDENCE
EMBEDDING TECHNOLOGY

herta security

FORTH
Institute of Computer Science

SECO

VIMAR
energia positiva


TECHNOLOGY INNOVATIONS
• Shared
• Distributed
• Modular & scalar
• Multiplatform
• High performance
• Low-cost/Low-power consumption
• Easy programmable & sustainable
• Usability & adaptability constrains
• Open Source
SMART GRID
SMART SURVEILLANCE
SMART LIGHTING
SMART PARKING
SMART HOME
SMART CARS
SMART TAGS
SMART ENERGY
SMART HEALTH
APPLICATIONS
KEY SCENARIOS
SOFTWARE
(Alghorithms & Programme Languages)
EASY PROGRAMMABILITY
CYBER PHISICAL SYSTEM
ACCELERATING FUNCTIONS
EMBEDDED MODULAR SYSTEM
SENSING
Accelerometer
Magnetometer
Gyroscope
Pressure
Altimeter
Temperature etc.
EMBEDDED PROCESSING
MCU
MPU
Hybrid MCU/MPU
Network Processor
CONNECTIVITY
NFC
6LoP AN
Sub-Gig
ZigBee
GPS
BT/BTLE
Wi-Fi
RFID
Cellular

FUTURE AND EMERGING TECHNOLOGIES
6.13 Meuro funding 2010-13

Exploiting Dataflow Parallelism in Teradevice Computing

TERA^{F}LUX

http://teraflux.eu

Università di Siena
(Coordinator)

Barcelona
Supercomputing Center

INRIA

Contact: Prof. Roberto Giorgi (project coordinator): http://www.dii.unisi.it/~giorgi

University of Augsburg

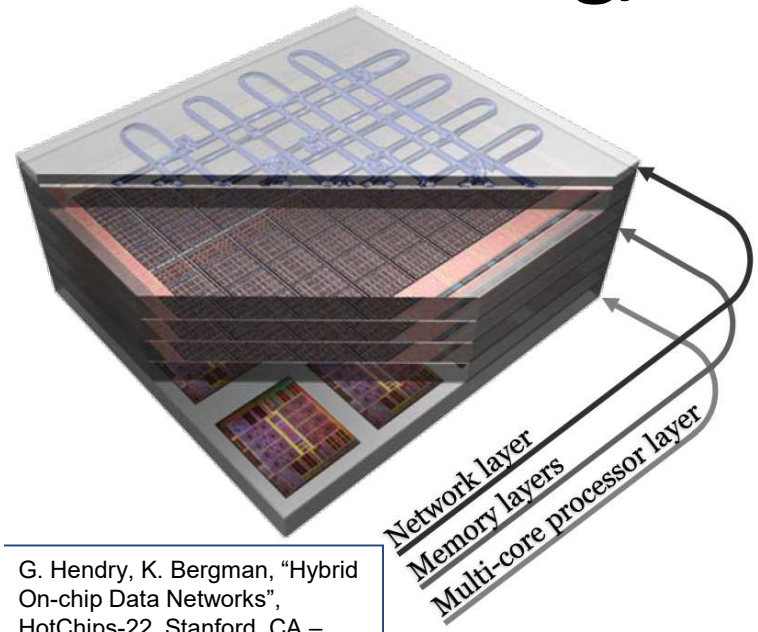
University of Manchester

University of Cyprus

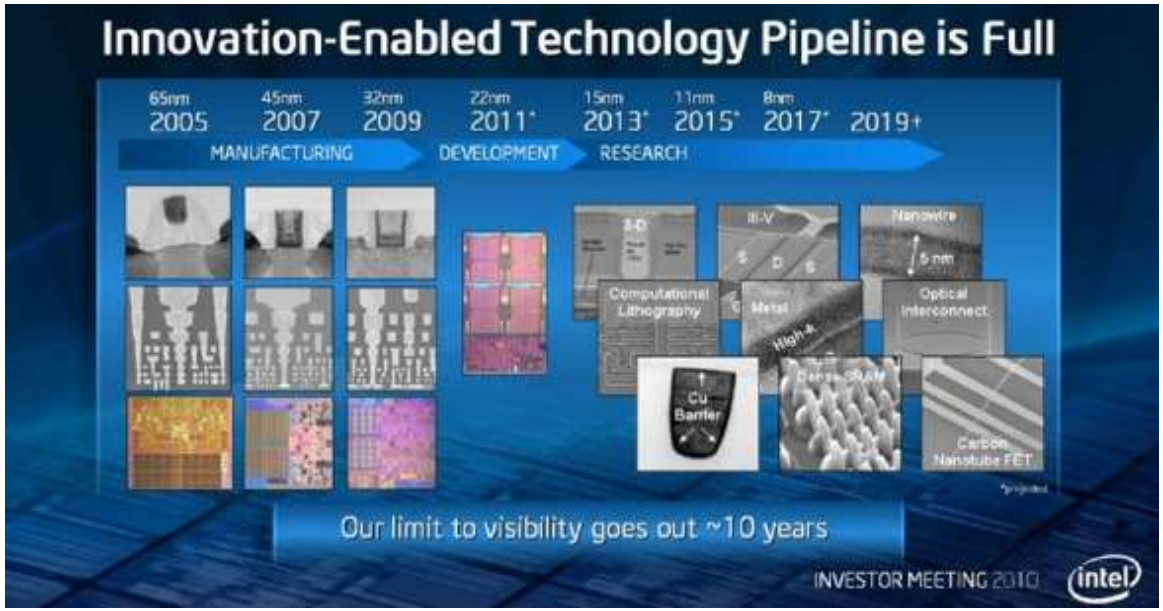
University of Delaware (USA)

(Nearer) Future Scenarios

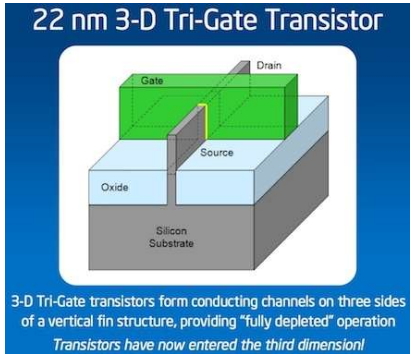
== 3D stacking, 8nm, 3D transistors, Graphene

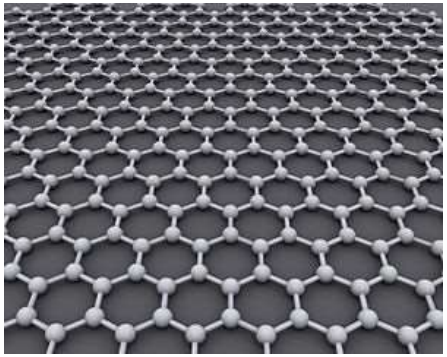


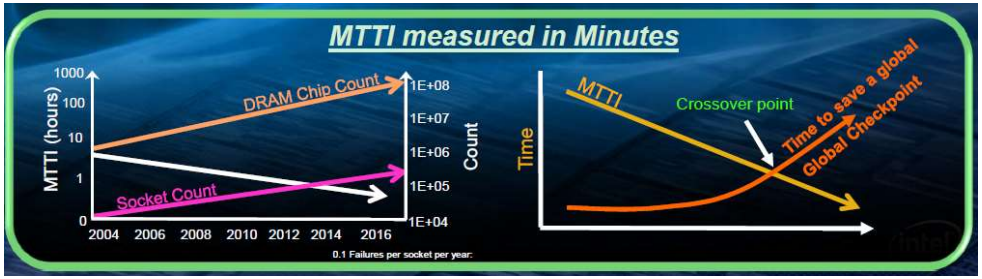
G. Hendry, K. Bergman, "Hybrid On-chip Data Networks", HotChips-22, Stanford, CA – Aug. 2010



Fab D1X (OR), 42 (AZ), 24 (Ireland) starting the 14nm node in 2013







Pawloski, May 2011, Exascale Seminar, Ghent

ERA Embedded Reconfigurable Architectures

Project number: 249059

FP7 – 2010-2013 -- ~ 3 Meuro funding

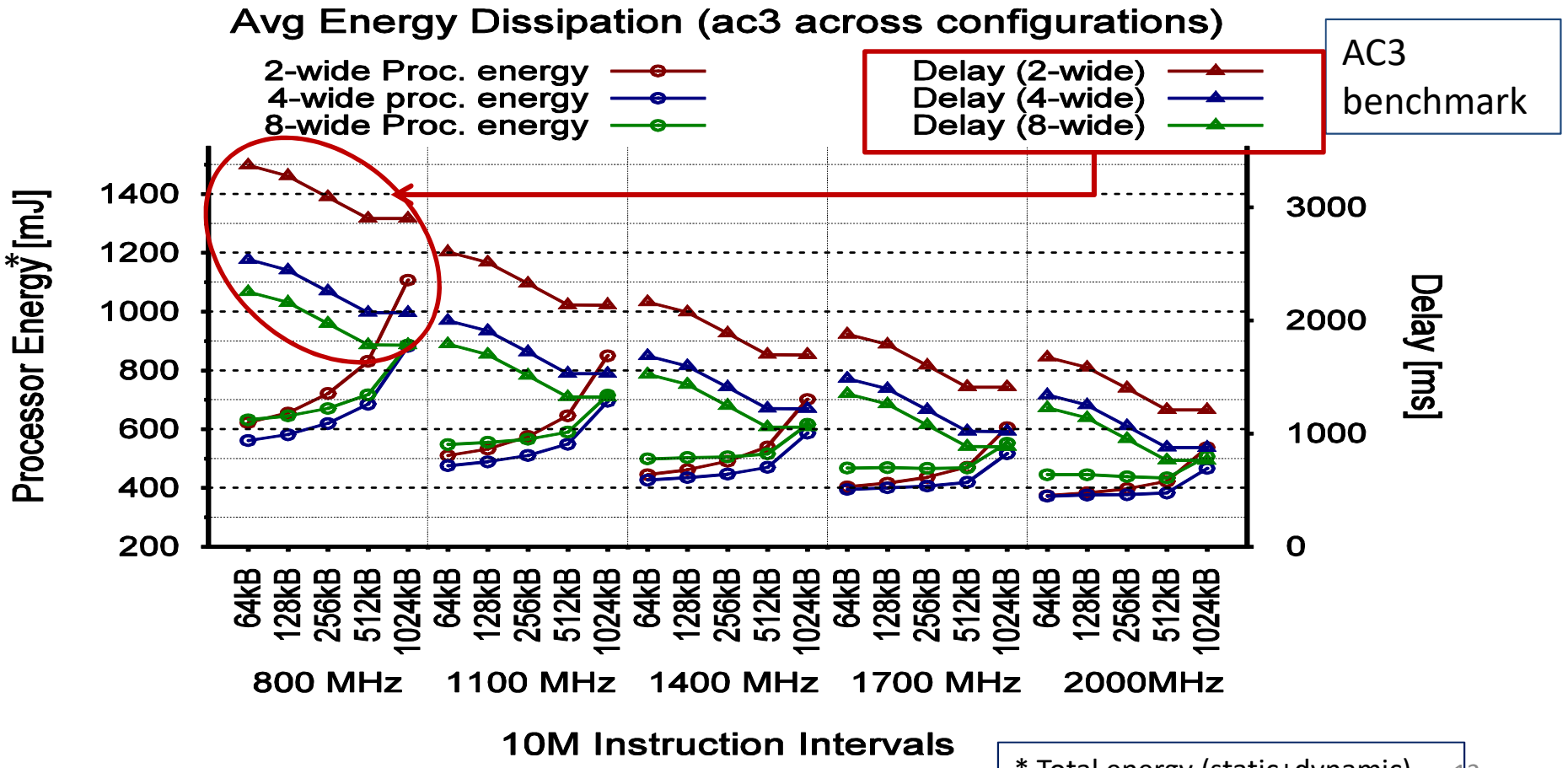
ERA TARGET SYSTEM

- Smartphone with FPGA-based SoCs (e.g Zynq)
- Exploring the energy efficiency of reconfigurable hardware

Xilinx Virtex6

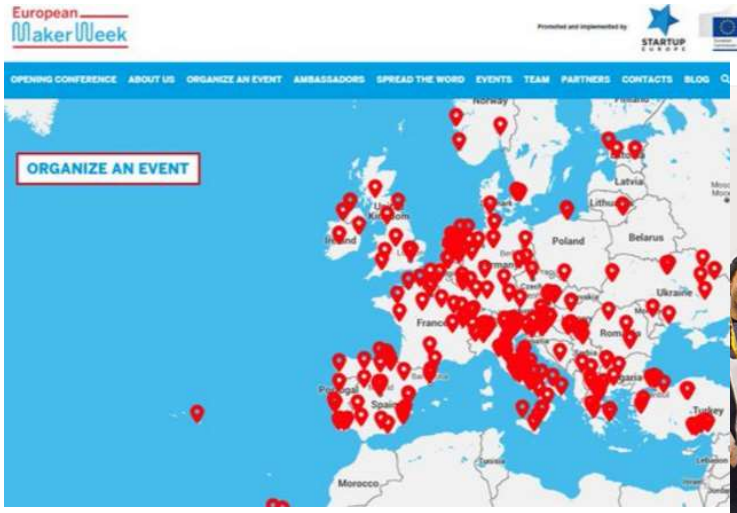
Benchmarks analysis from energy+delay viewpoint

- **DYNAMYC ENERGY** consumption and **DELAY** while varying L2 cache-size, issue-width, frequency
- Delay significantly decreases with L2 cache size, frequency, issue-width (total energy as in previous slide)
- These behaviors have been confirmed across all the EBS applications

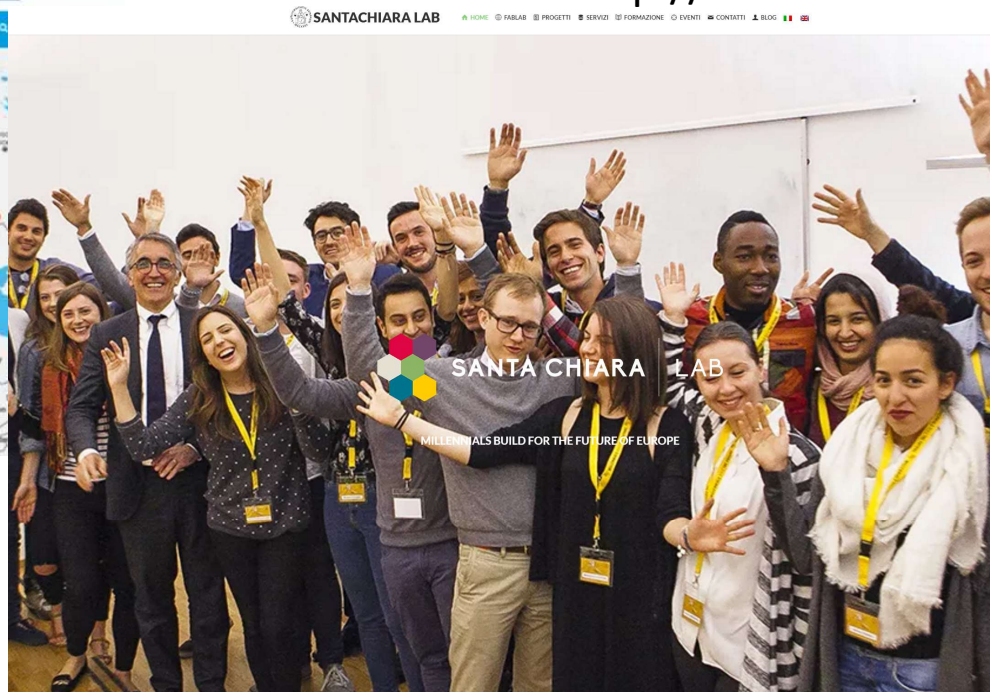


* Total energy (static+dynamic)

Cooperation with SantaChiaraLab (100m from us), Dept. Cognitive Science (in-building) & SECO (Arezzo)



http://santachiaralab.unisi.it/



UDOO X86 FOR CLUSTER

SECO/UNISI achievements:

- 2014: UDOO-ARM (99 $ PC+Arduino) → 600k$ on Kickstarter
- 2016: UDOO-x86 (PC+Arduino, 10x faster than Raspberry-3) → 800k$ on Kickstarter
- Selected among the finalists of the EU “Innovation Radar Prize” (Sep. 2016)

POWERED BY OmpSs
THANKS TO AXIOM

UNIVERSITY OF SIENA – ROBERTO GIORGI

Thanks
for your attention!