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Luigi Raffo[1], Eduardo de la Torre[1]
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Providing Advanced Adaptivity in Cyber-Physical Systems with Multi-Grain Reconfiguration

Horizon 2020
European Union funding
for Research & Innovation

Outline

- Concepts & Definition
  - The Adaptation Loop
- Adaptive CPS: The CERBERO approach
  - Self-Adaptation in CERBERO H2020
  - Adaptation Fabrics in CERBERO H2020
- HW Adaptation in CERBERO
  - ARTICo3
  - MDC-compliant CG adaptation
- Mixed-Grain Adaptivity
  - ARTICo3 + MDC integration
- Assessment & Conclusion
  - Results on the PoC
  - Best of Both
  - Next Step

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CERBERO Goal

Cross-layer modEl-based fRamework for **multi-oBjective** dEsign of **Reconfigurable** systems in **unceRtain hybRid** envirOnments

(**CERBERO**)

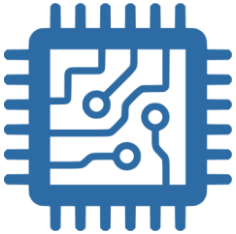
Integrated model-based *methodology* and initial *framework* for multi-objective design, incremental prototyping and continuous DevOps of *Adaptive Cyber Physical Systems*

- *From* (User Requirements)
- SoS and System level
- Application / Service level
- Real Time Manager level
- *To* Real Time Software and Hardware implementation

Self-Adaptation in Cyber-Physical Systems

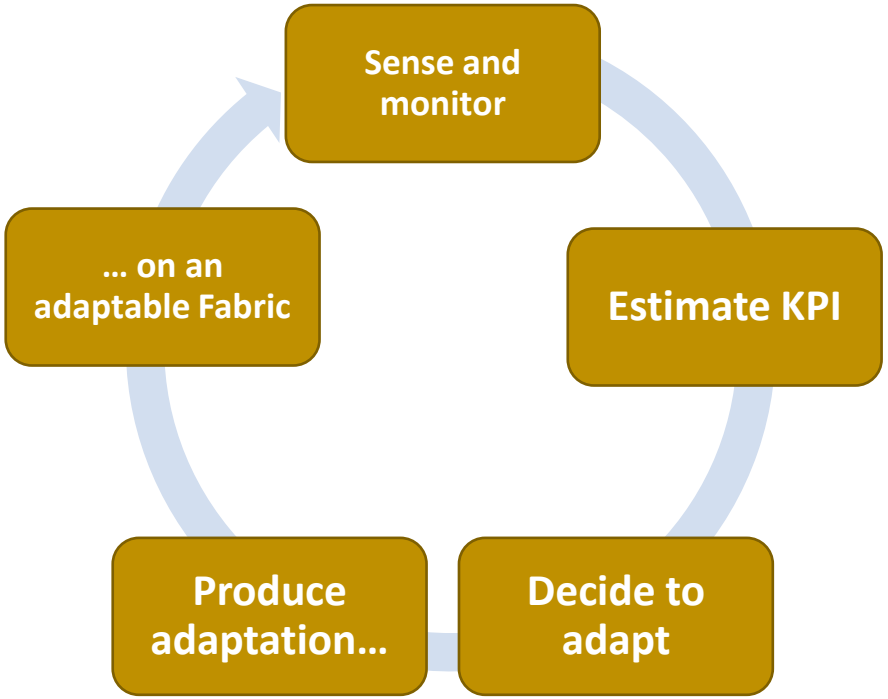
ENVIRONMENTAL AWARENESS: Influence of the environment on the system, i.e. daylight vs. nocturnal, radiation level changes, etc.
Sensors are needed to interact with the environment and capture conditions variations.

USER-COMMANDED: System-User interaction, i.e. user preferences, etc.
Proper human-machine interfaces are needed to enable interaction and capture commands.



SELF-AWARENESS: The internal status of the system varies while operating and may lead to reconfiguration needs, i.e. chip temperature variation, low battery.
Status monitors are needed to capture the status of the system.

Adaptation Loop



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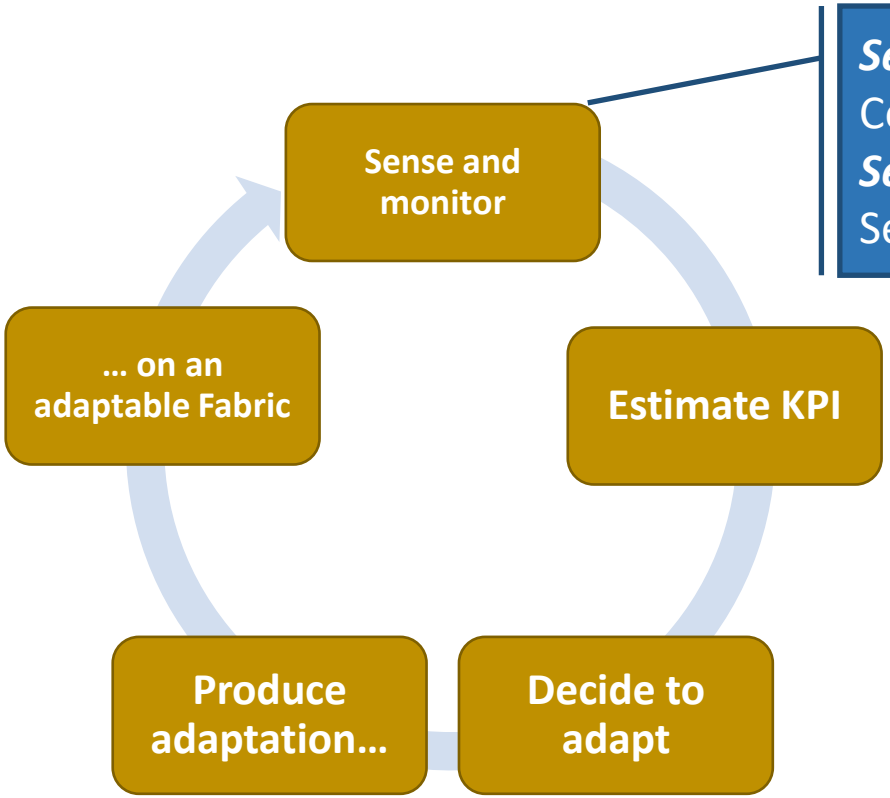
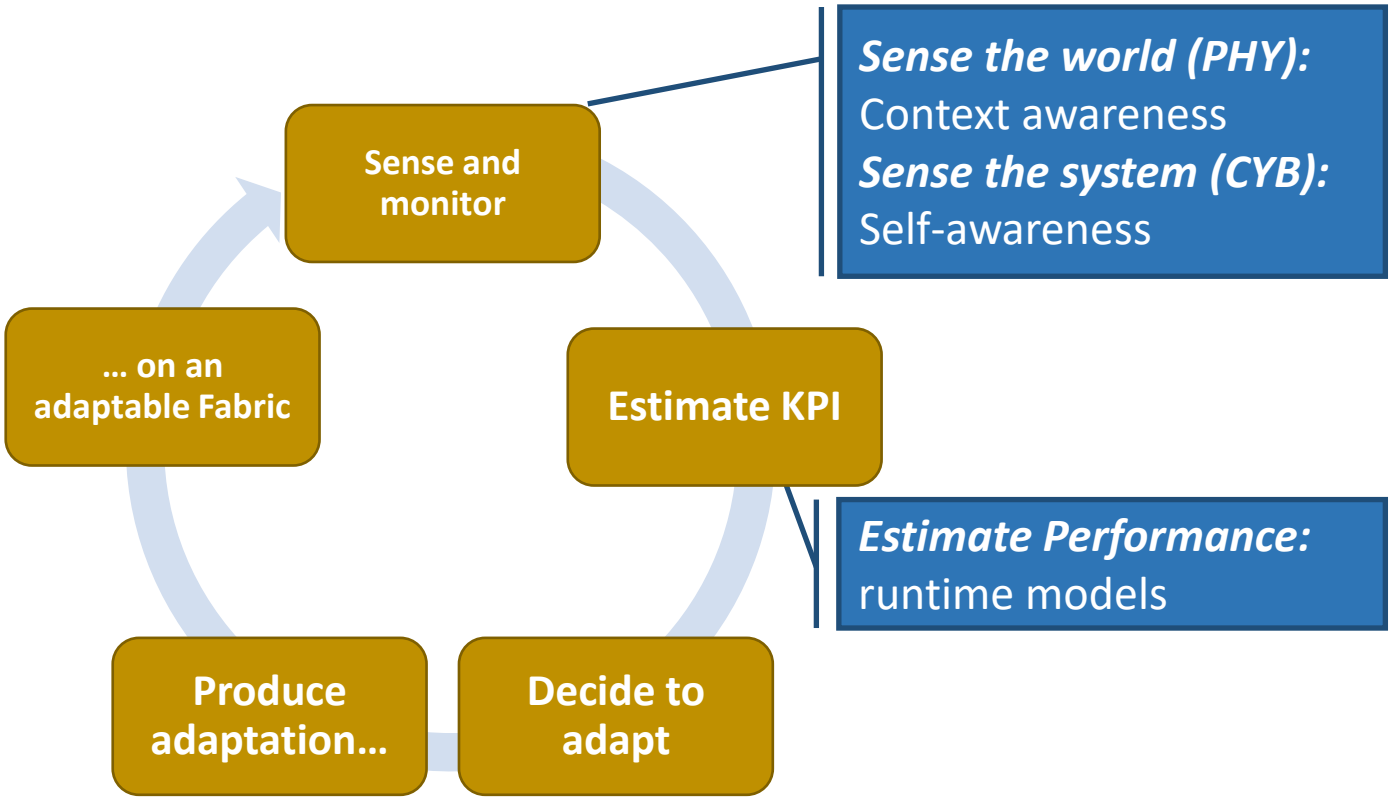


Sense the world (PHY):
Context awareness
Sense the system (CYB):
Self-awareness

Adaptation Loop



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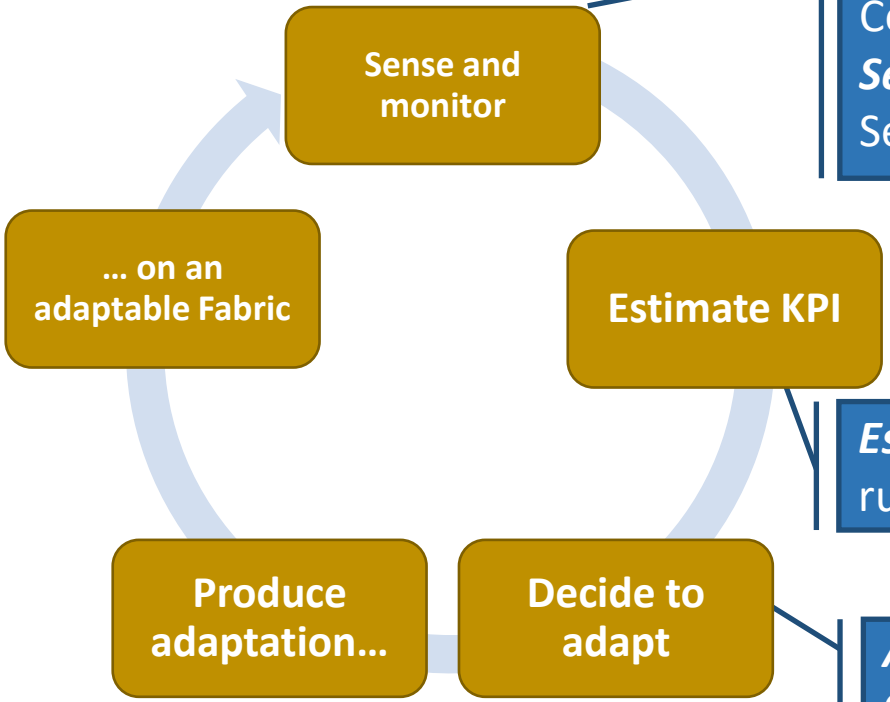

Sense the world (PHY): Context awareness
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Estimate Performance: runtime models

Analyse & Decide: Change task – Optimize - Repair

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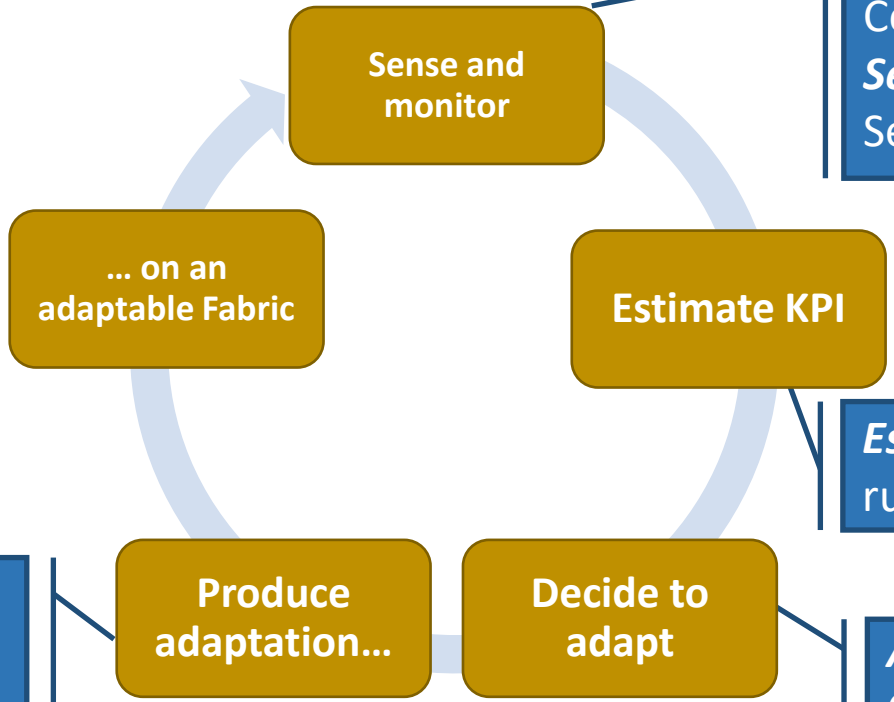

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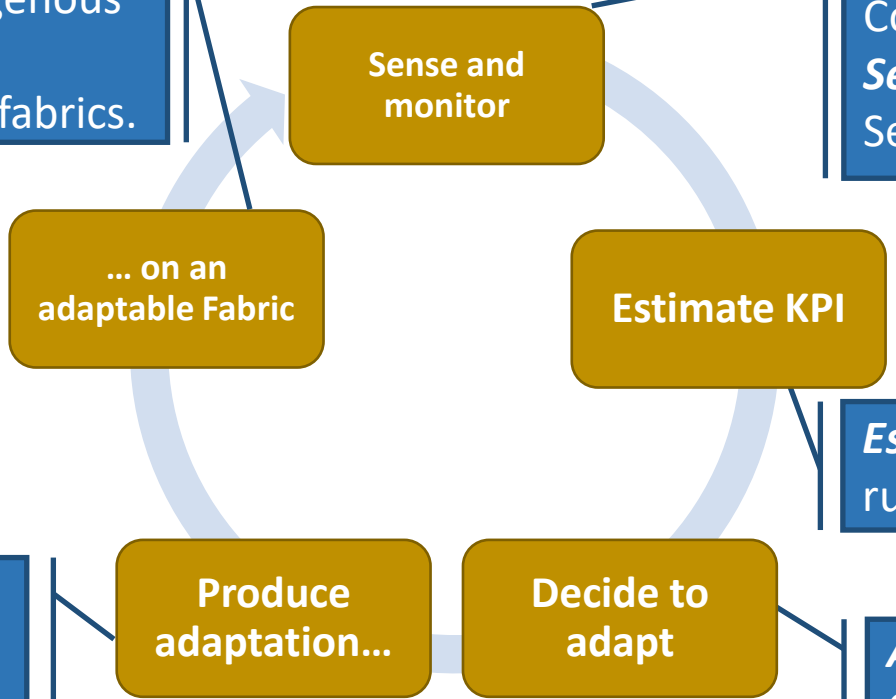

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Command Adaptation:
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Adapt:
Reconfigure the heterogenous (HW-SW) computing infrastructure. Multiple fabrics.

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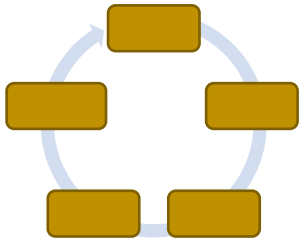

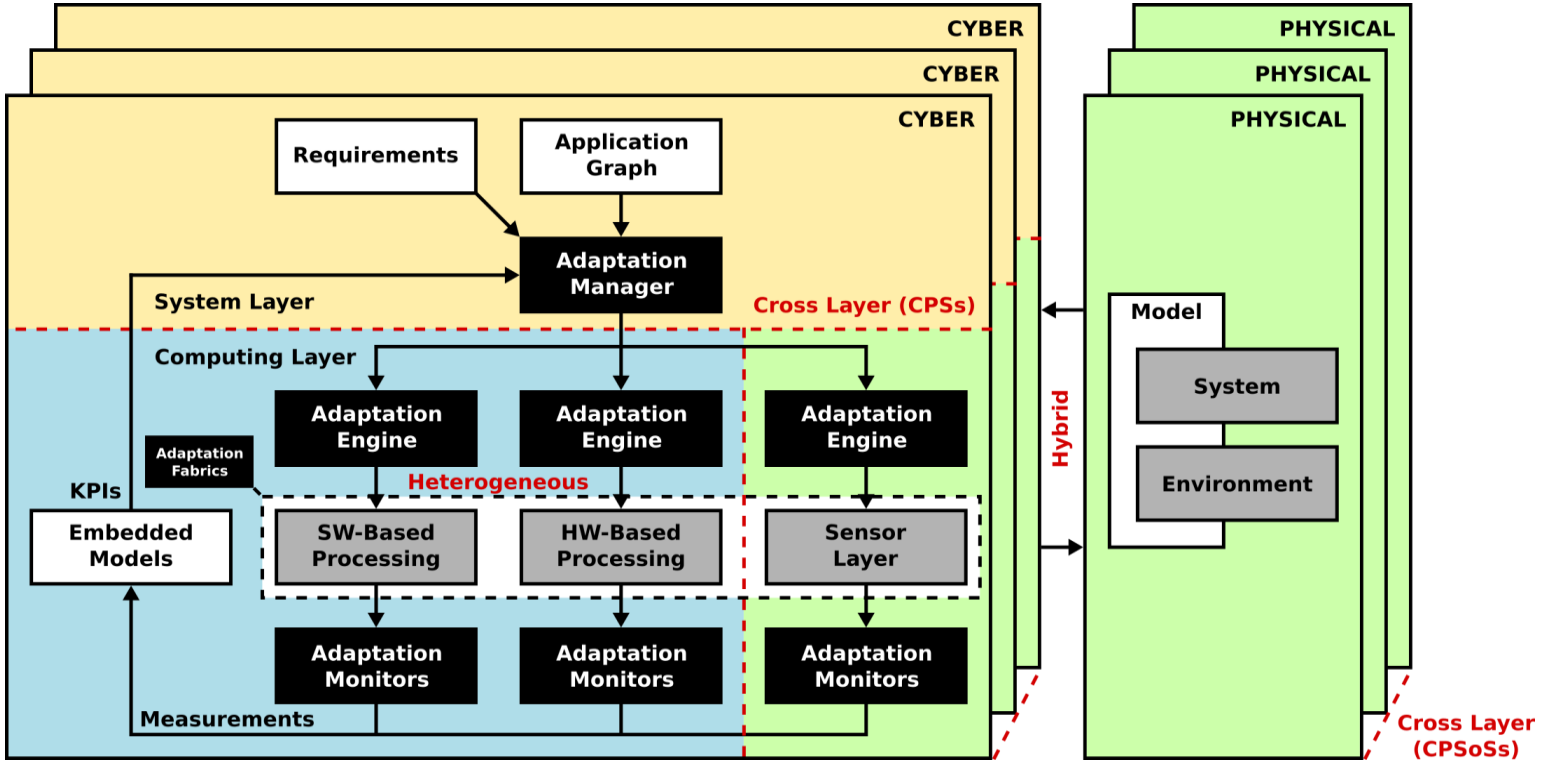

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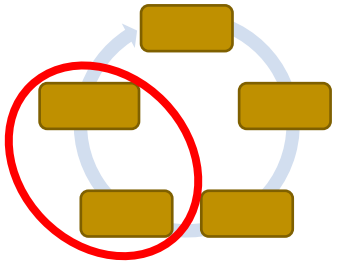

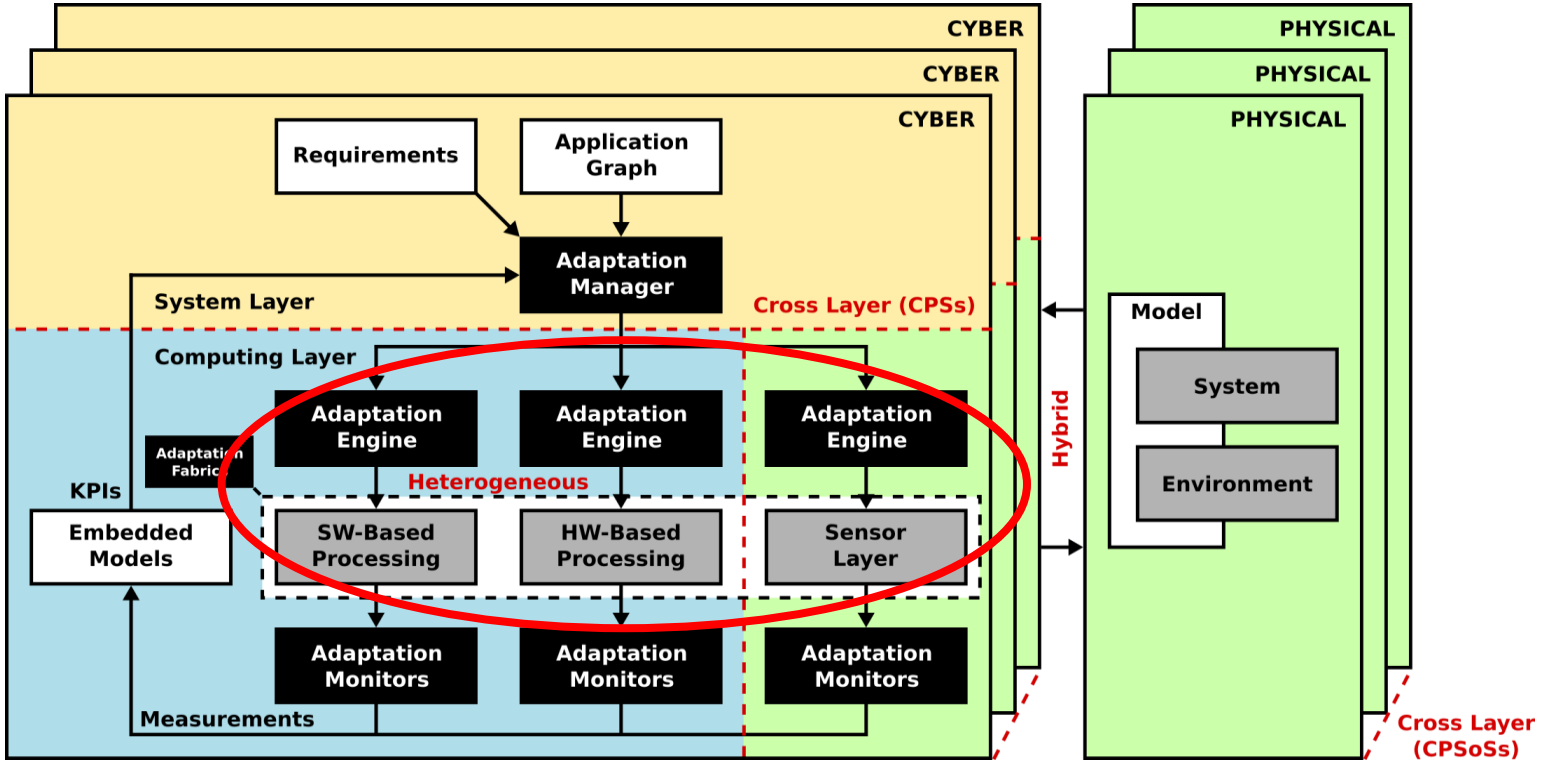

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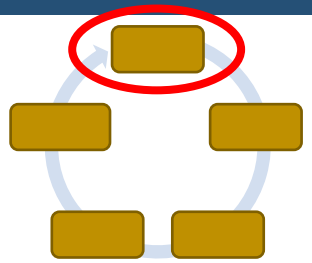

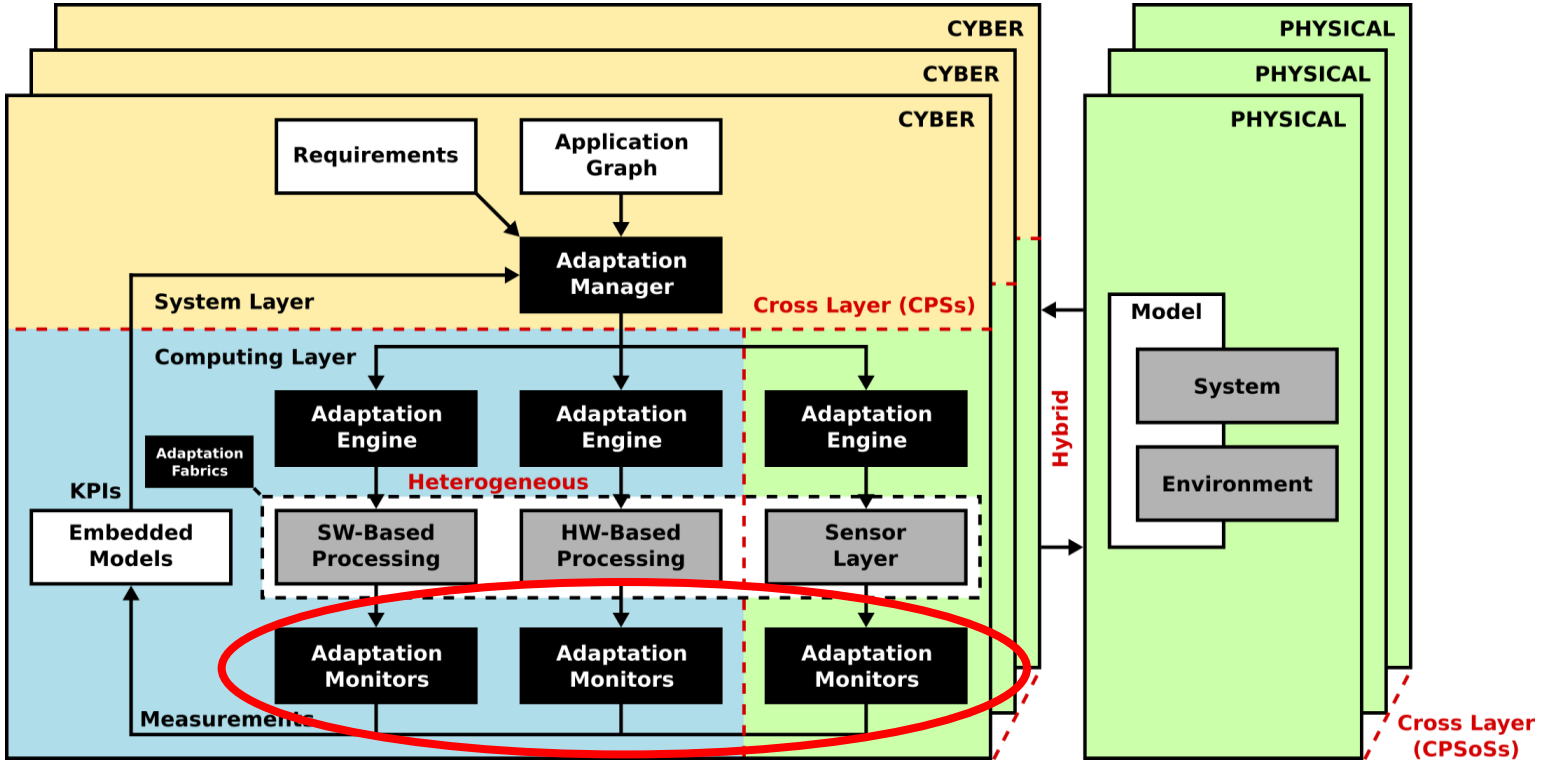

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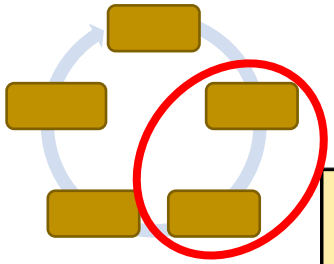
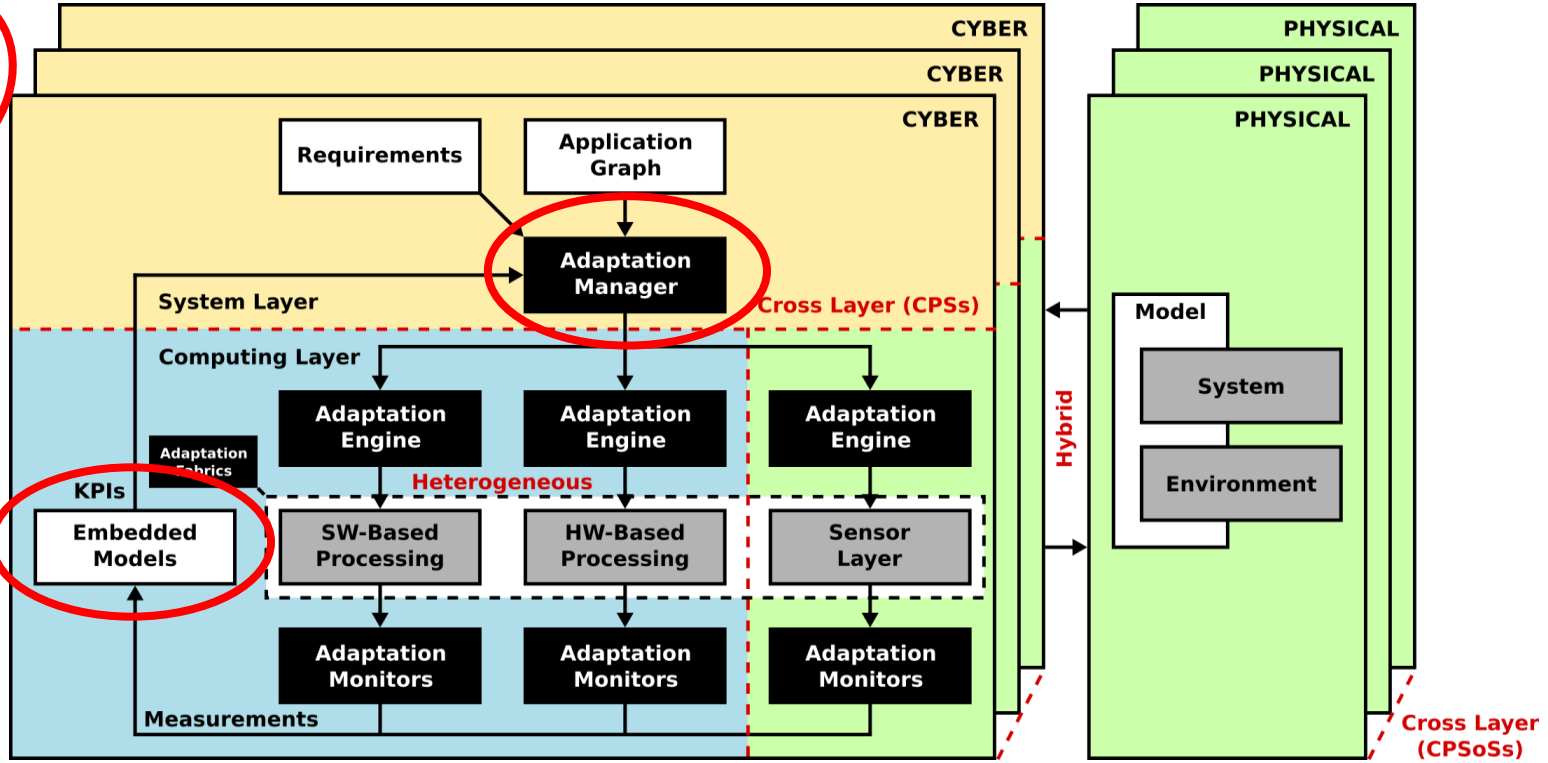
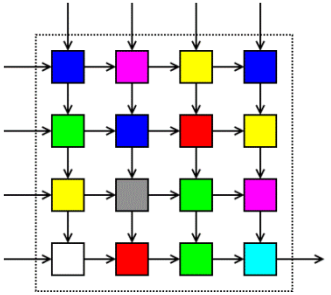




DPR & CG-VRC

DPR → *Dynamic and Partial Reconfiguration*

- Lower reconfiguration speeds
- Better operation speed (no mux/less logic)
- Better Resource Utilization (no dark logic)
- Higher Flexibility and Scalability
- Technology dependent (FPGA)



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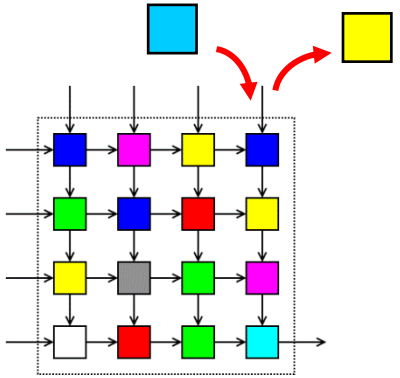

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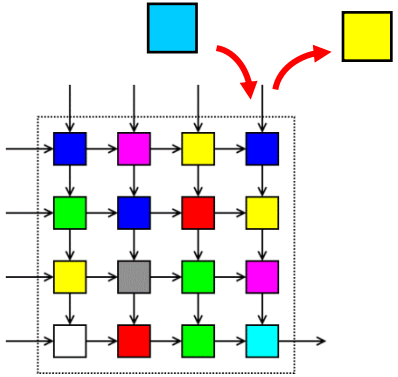

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- High reconfiguration speed
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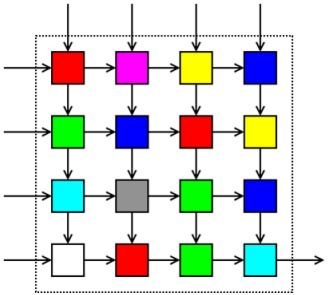
- Higher Area Overhead
- Technology independent (ASIC or FPGA)



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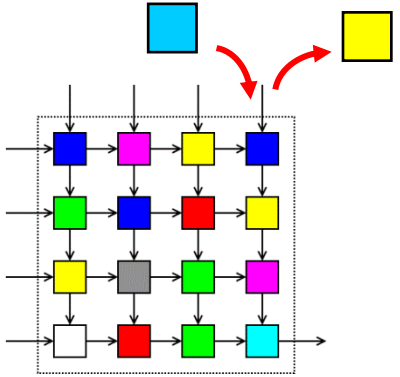

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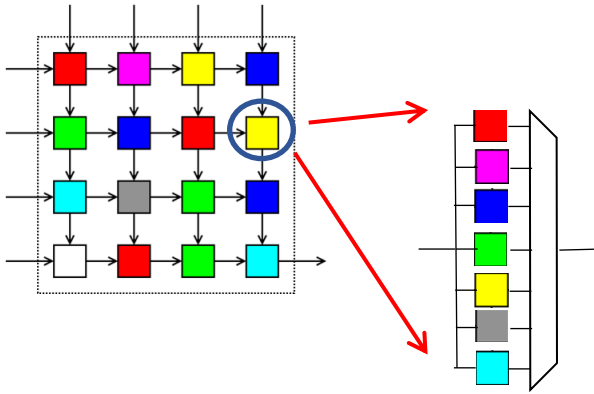

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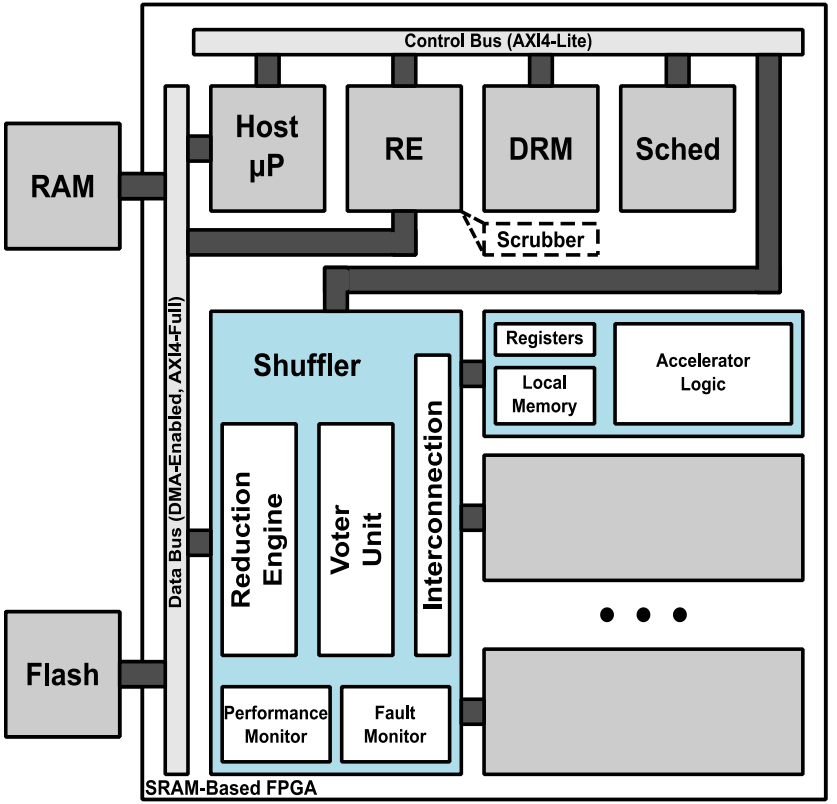

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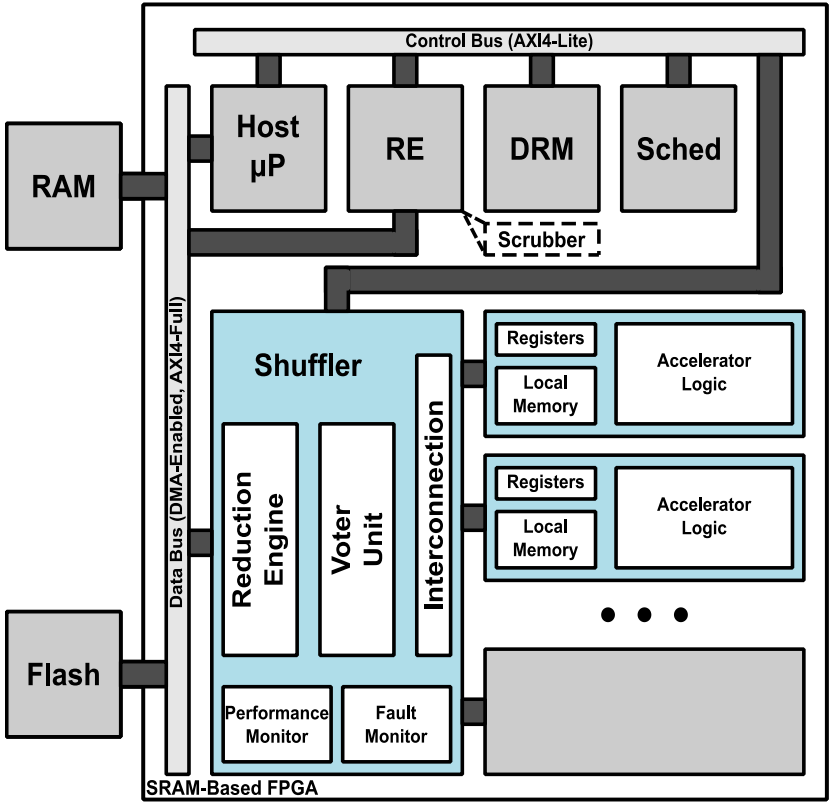

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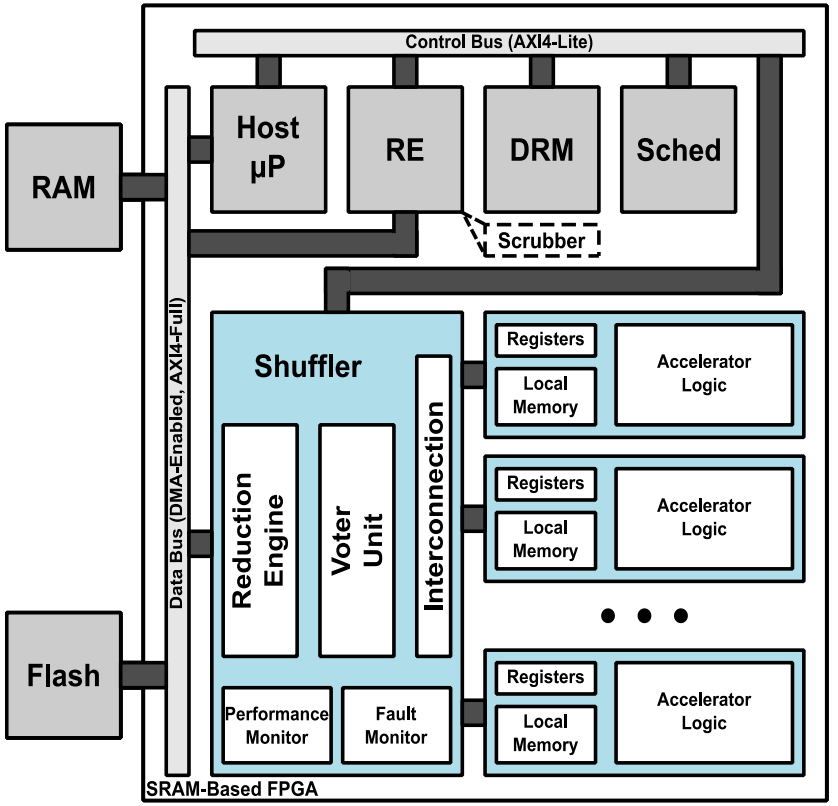

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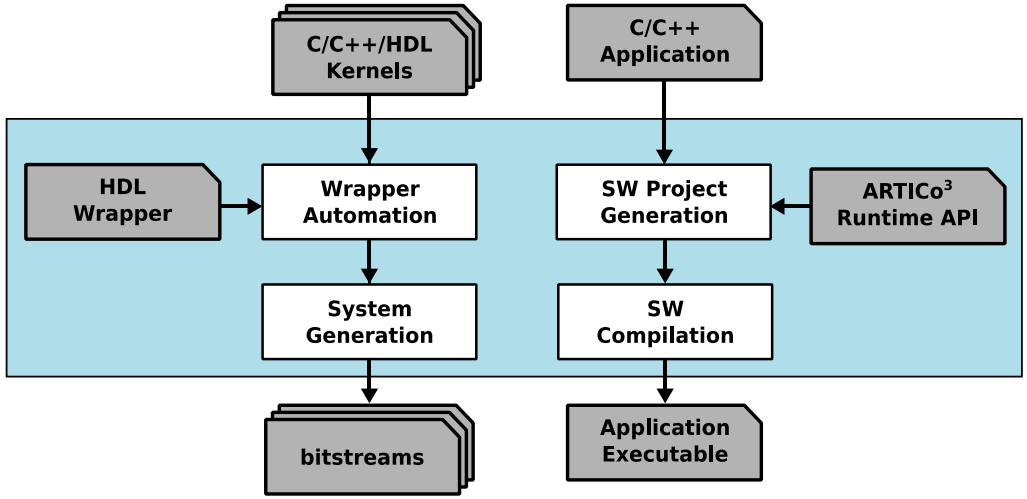

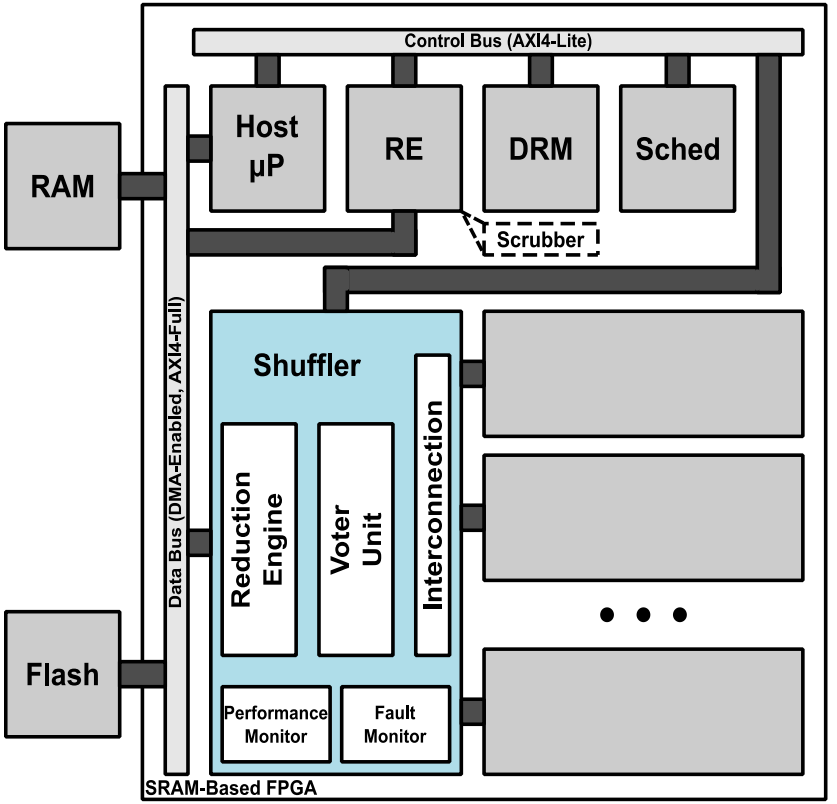

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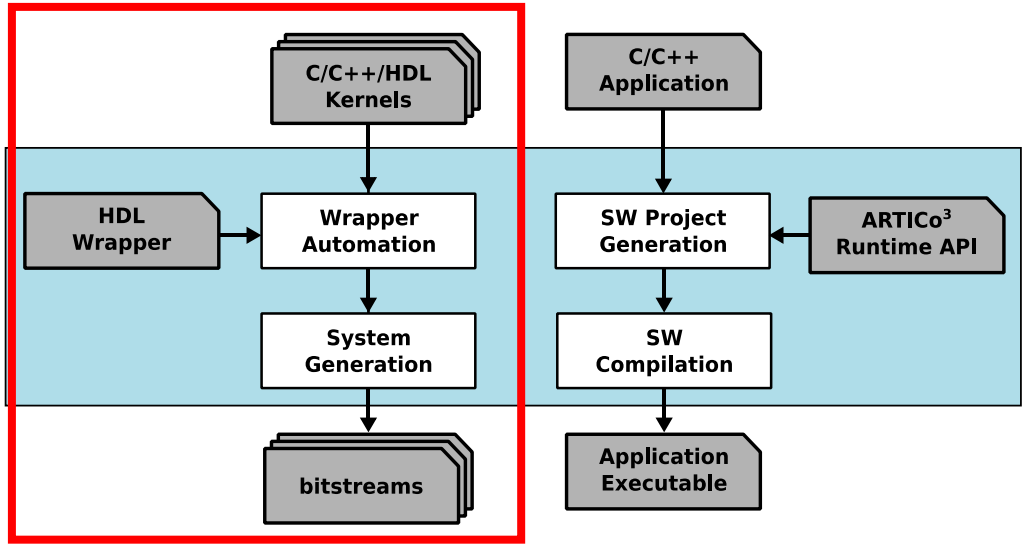

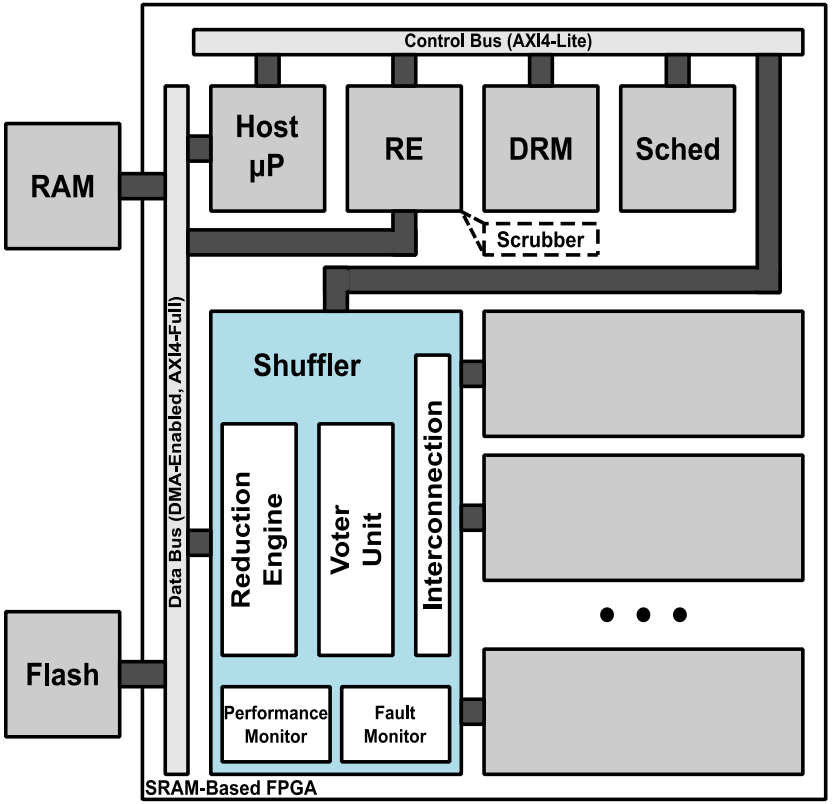

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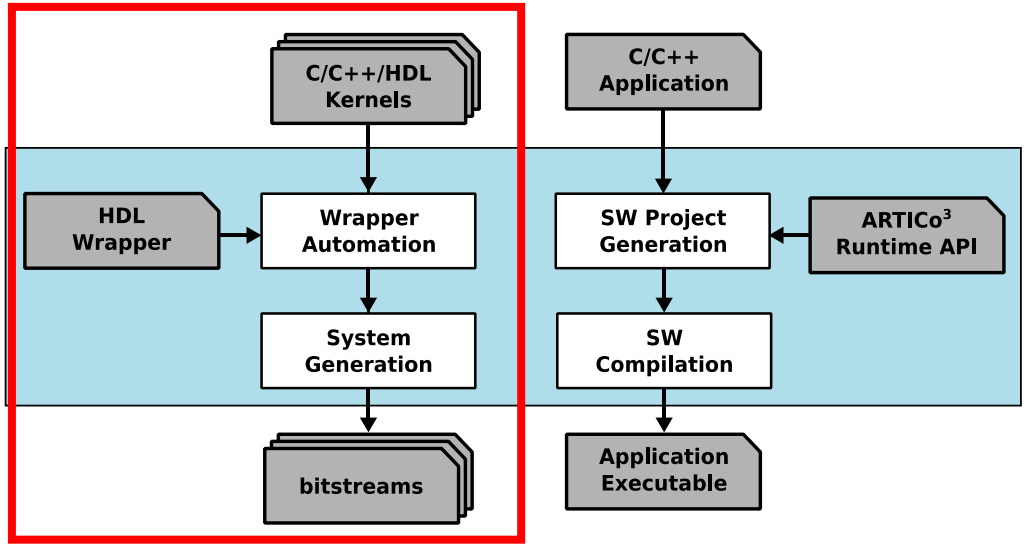

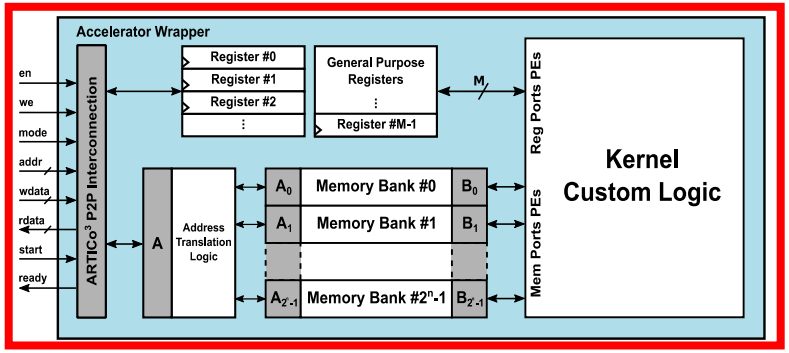

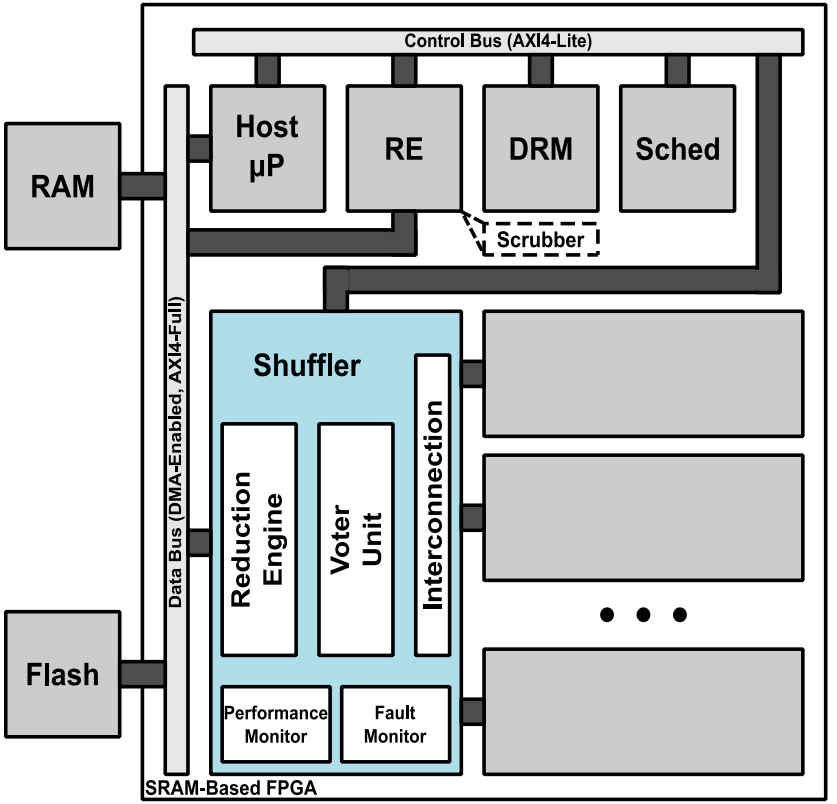

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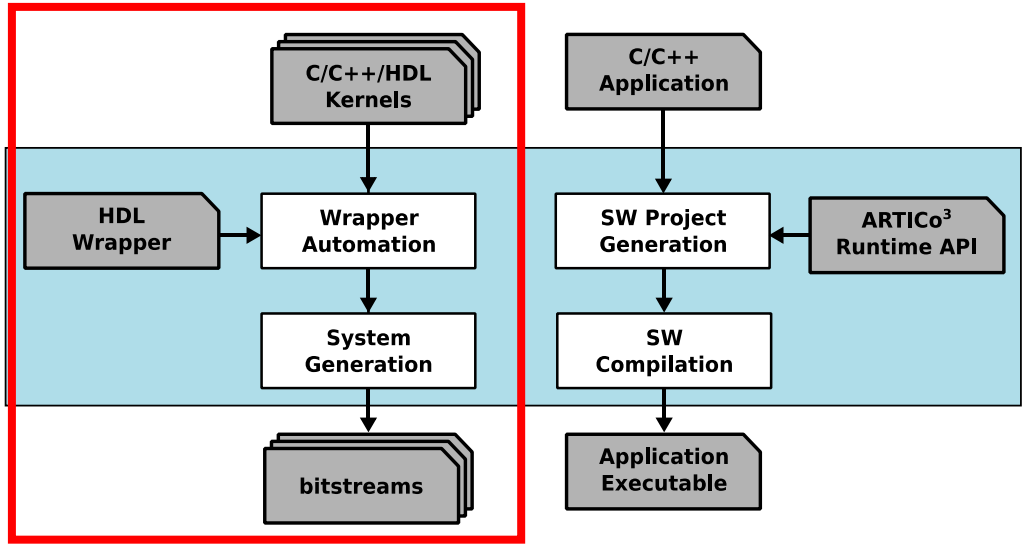

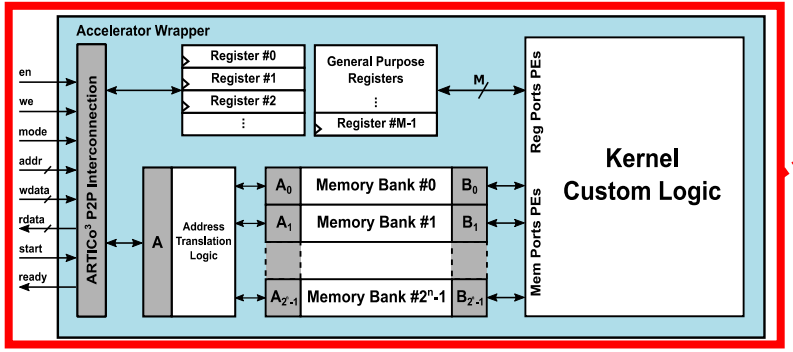

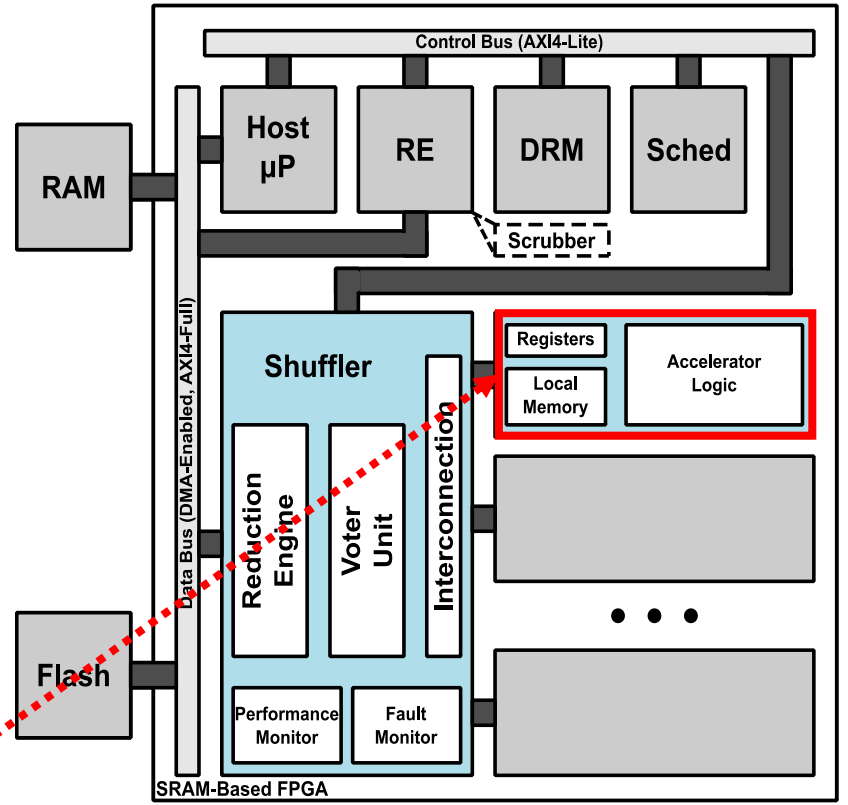

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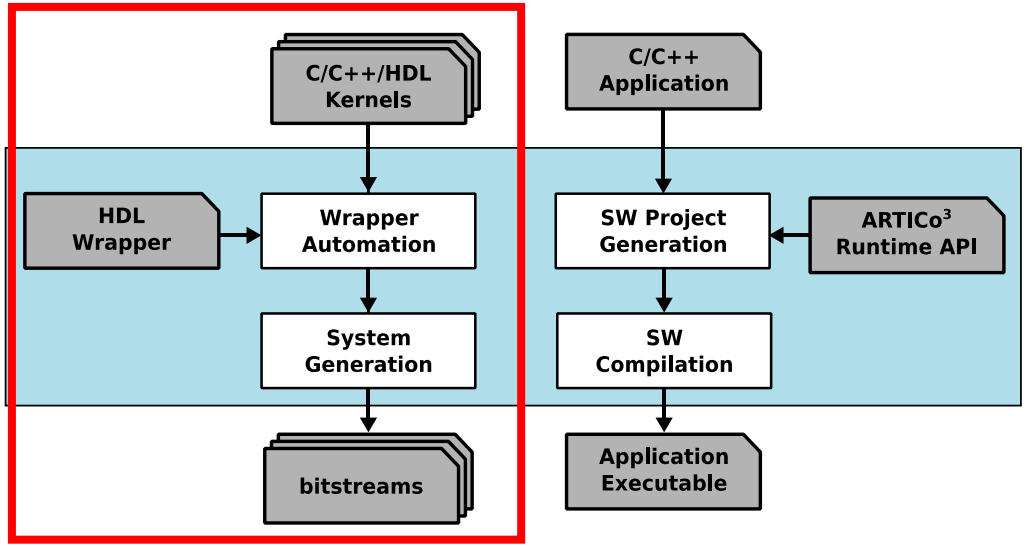

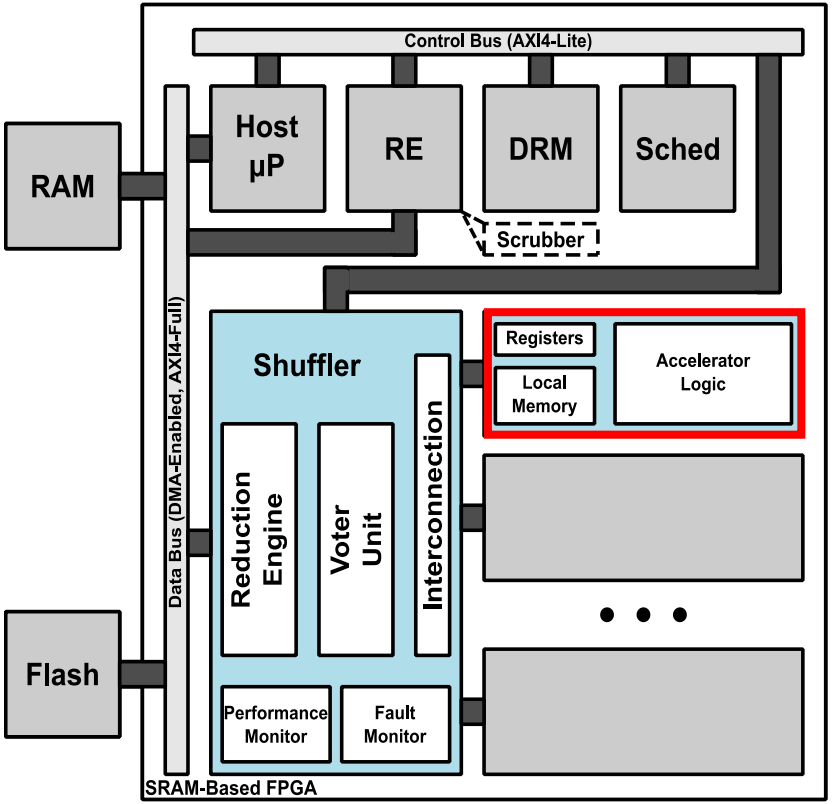

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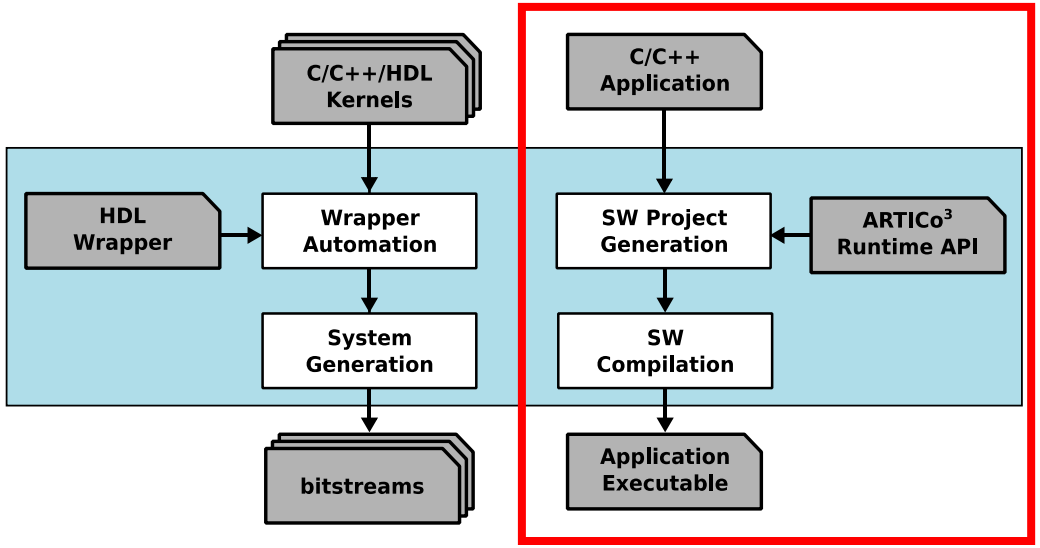

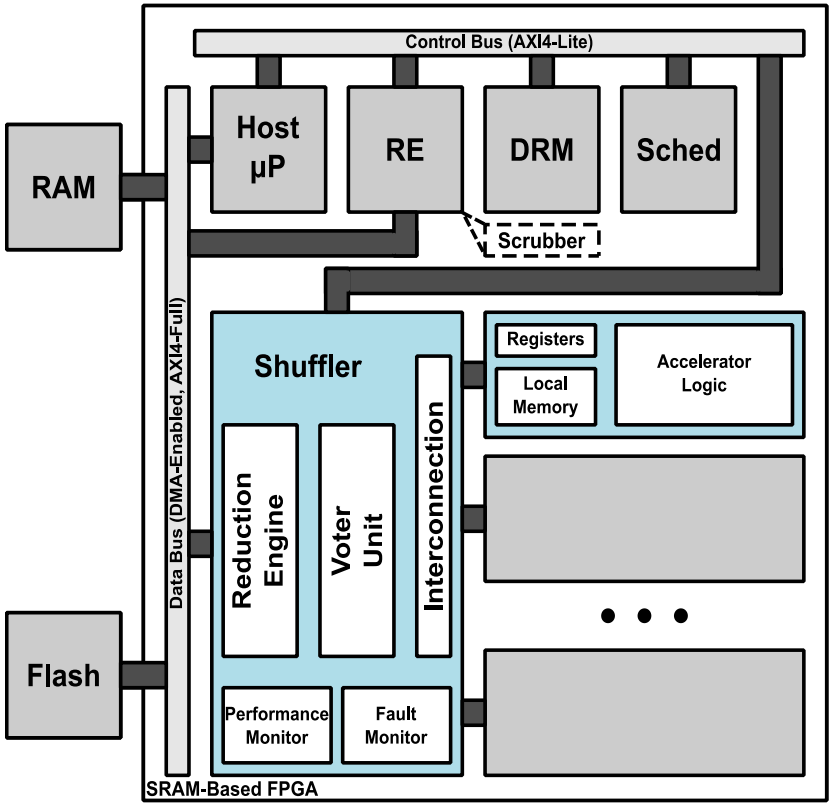

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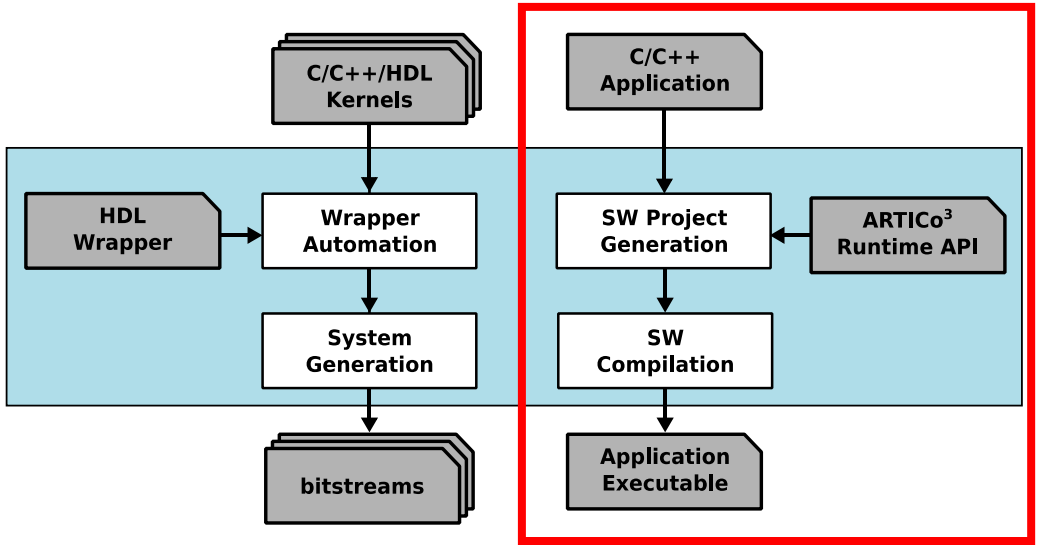

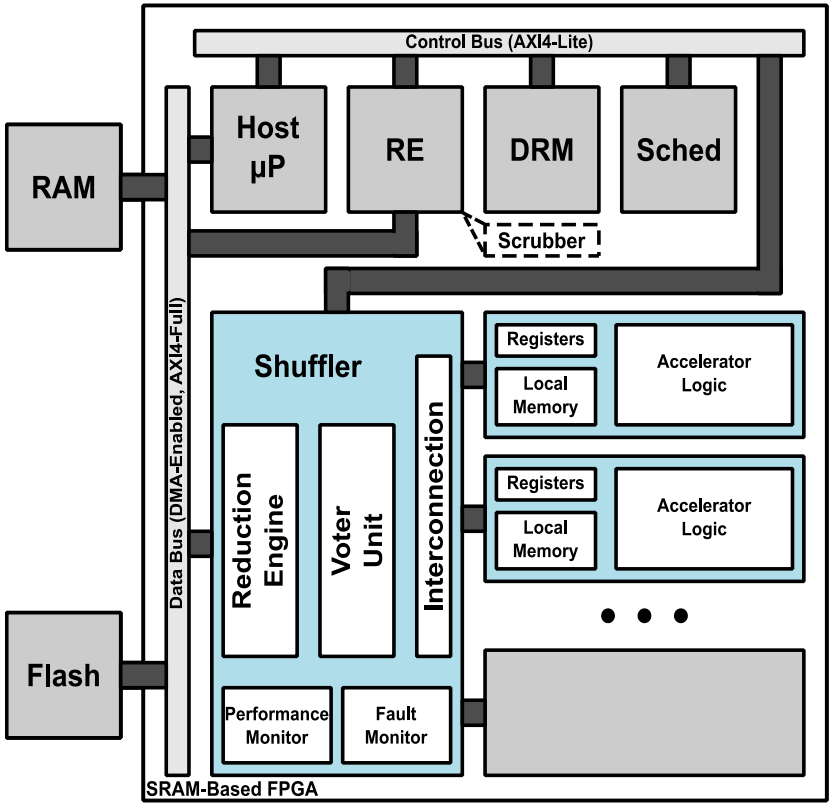

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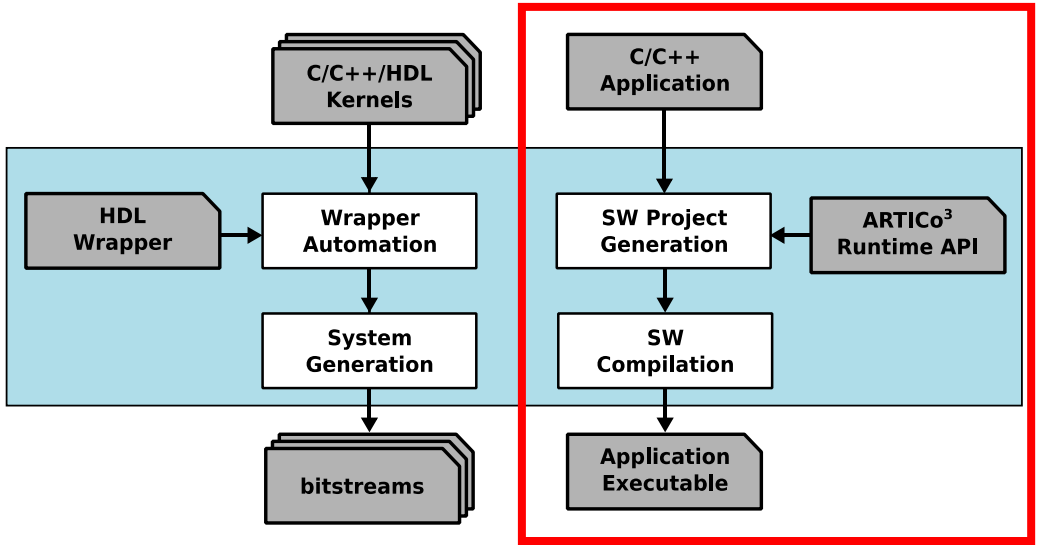
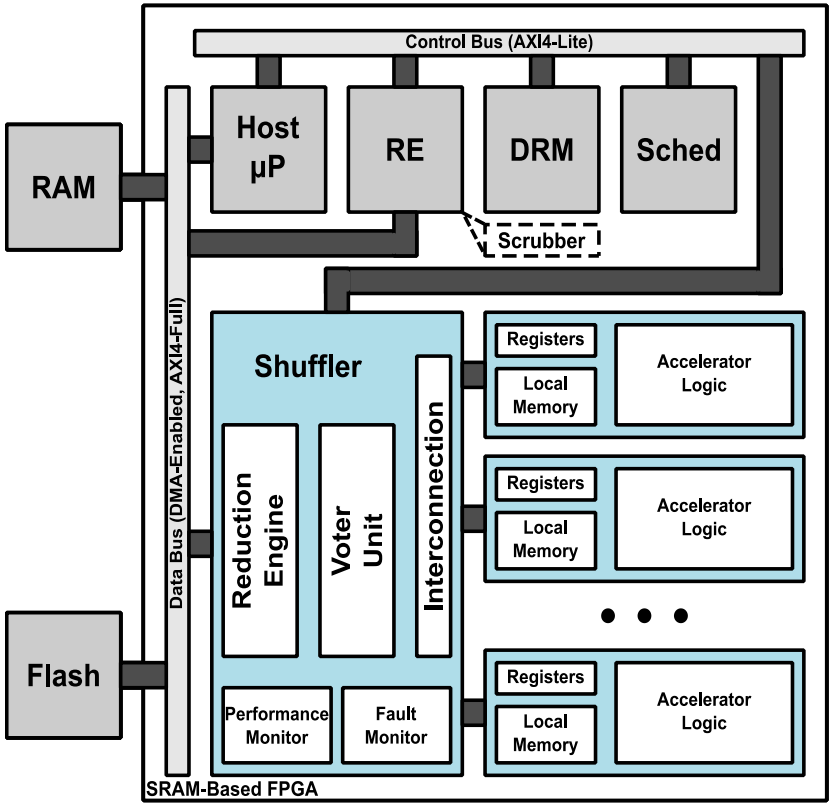
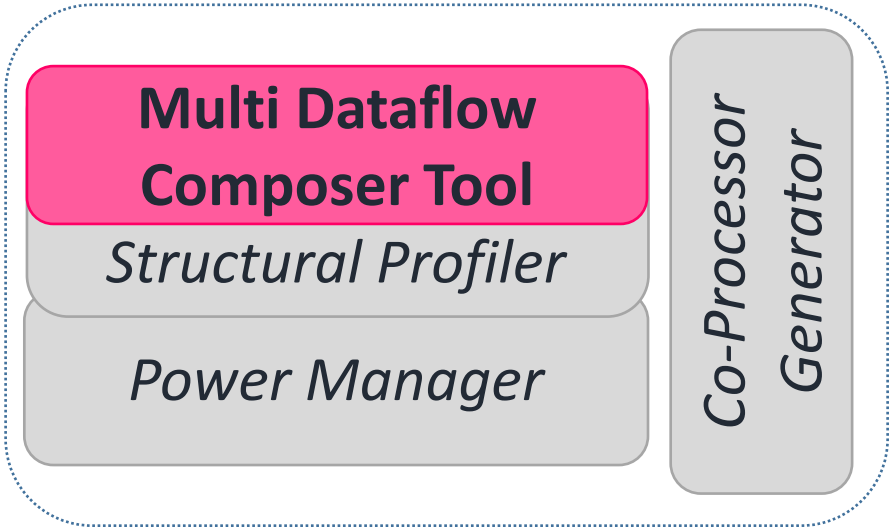


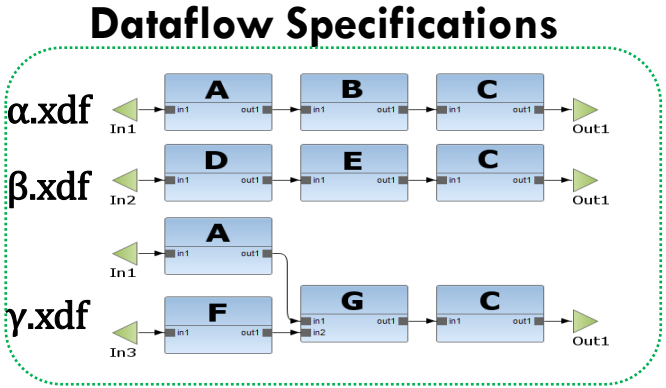


MDC tool: Dataflow to HW Mapping



MDC design suite

http://sites.unica.it/rpct/



MDC tool: Dataflow to HW Mapping

Multi Dataflow Composer Tool

Structural Profiler

Power Manager

Co-Processor Generator

MDC design suite

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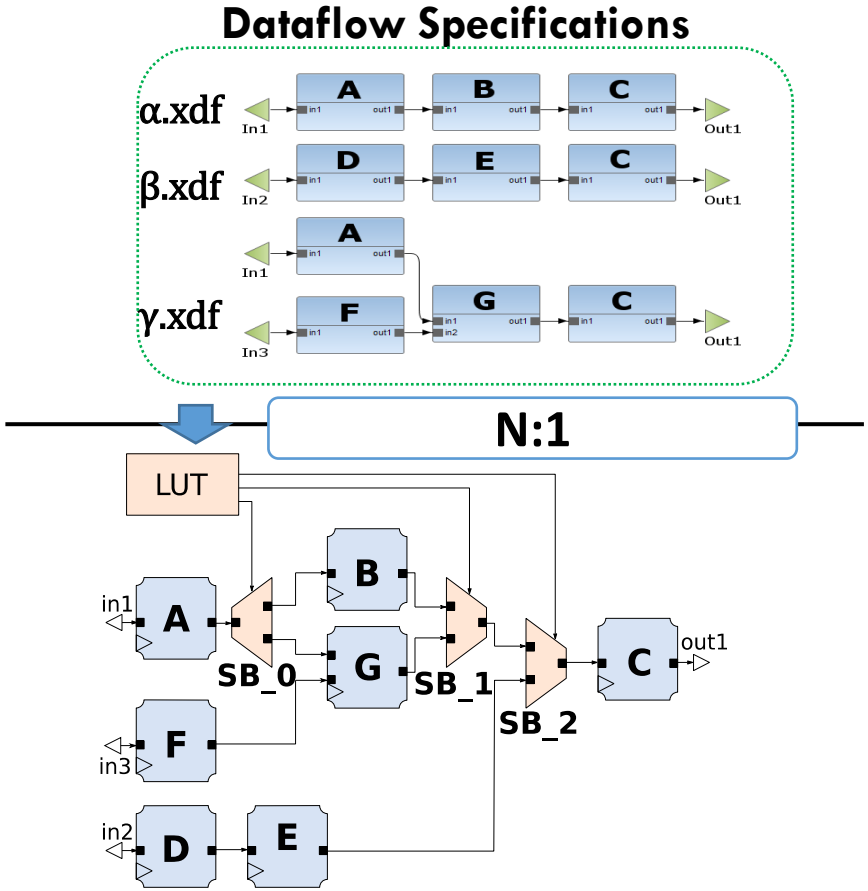

MDC Tool: Coprocessor Generator

Co-Processor Generator:

generation of ready-to-use Xilinx IPs

Multi Dataflow Composer Tool

Structural Profiler

Power Manager

Co-Processor Generator

MDC design suite

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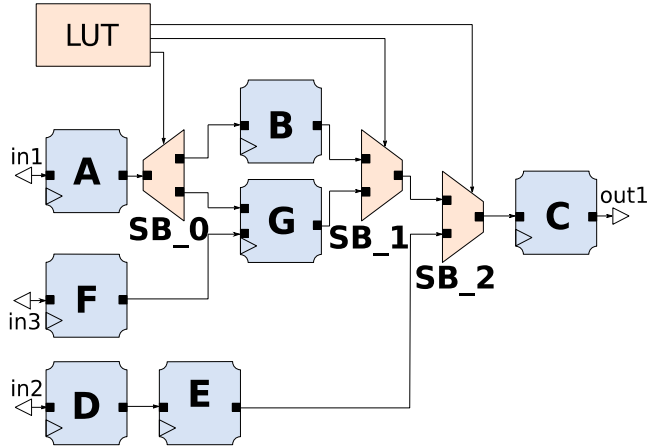

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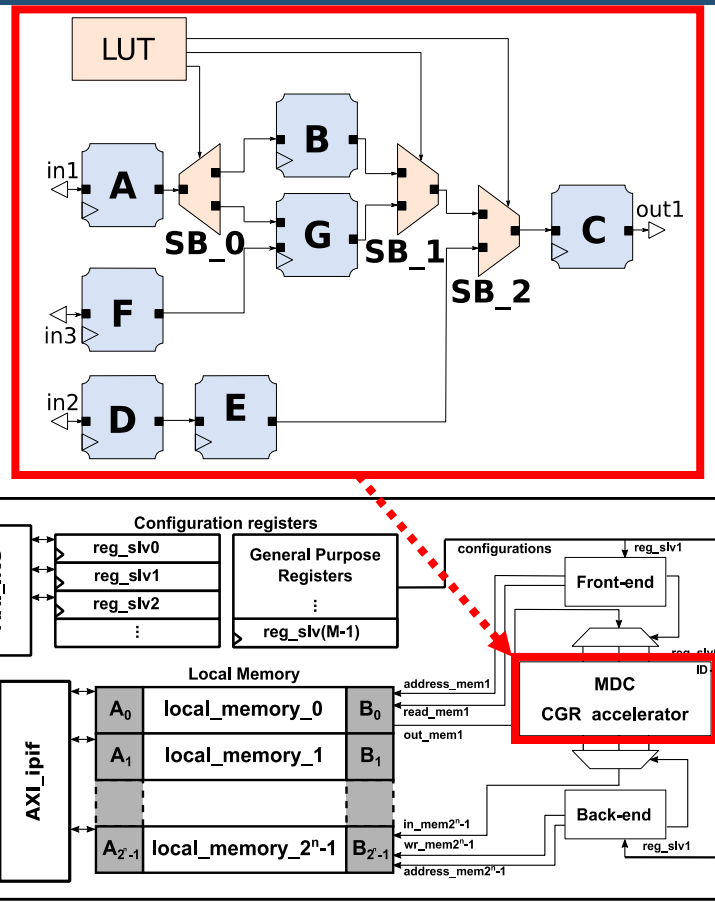

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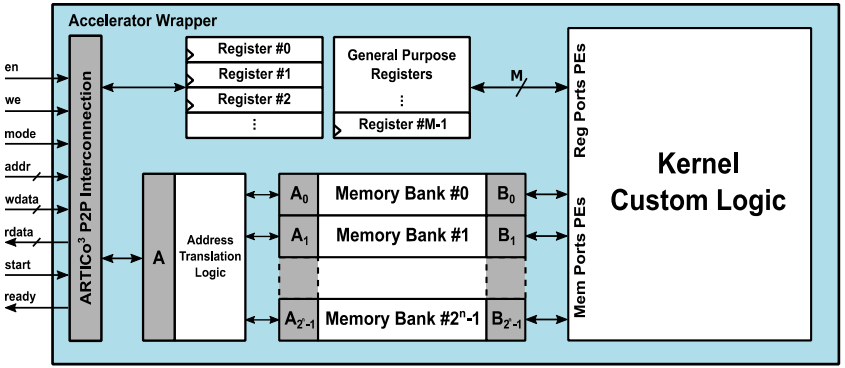
ARTICo³ + MDC: Kernels Adaptation

ARTICo³ slot wrapper



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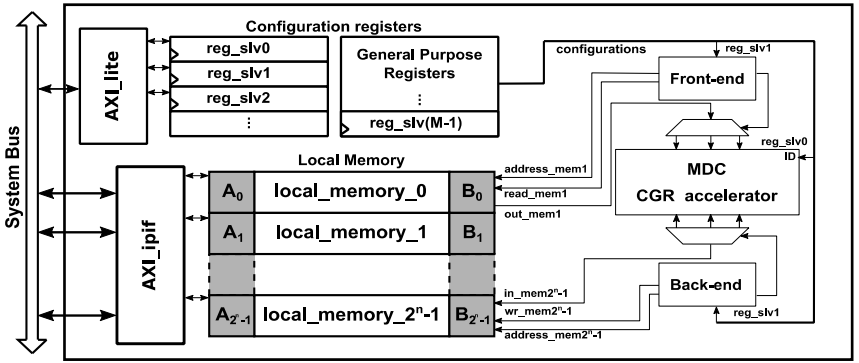

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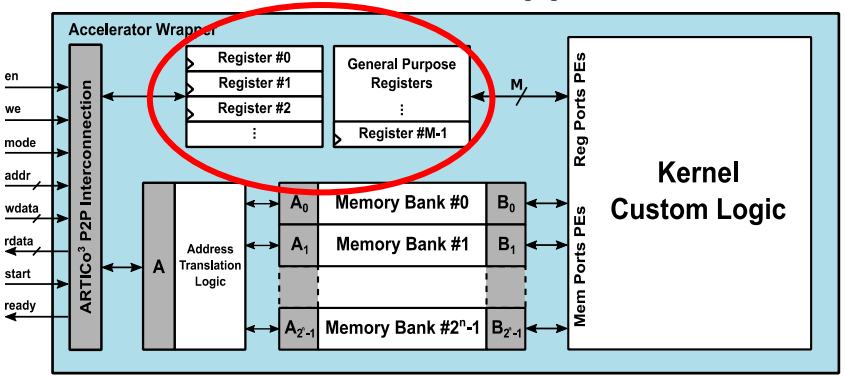

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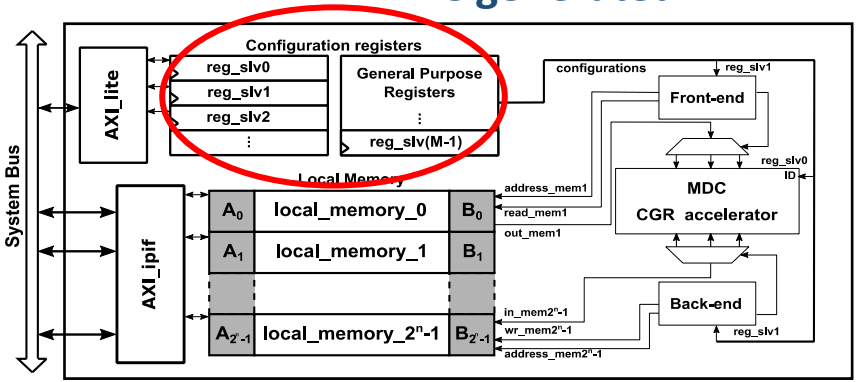

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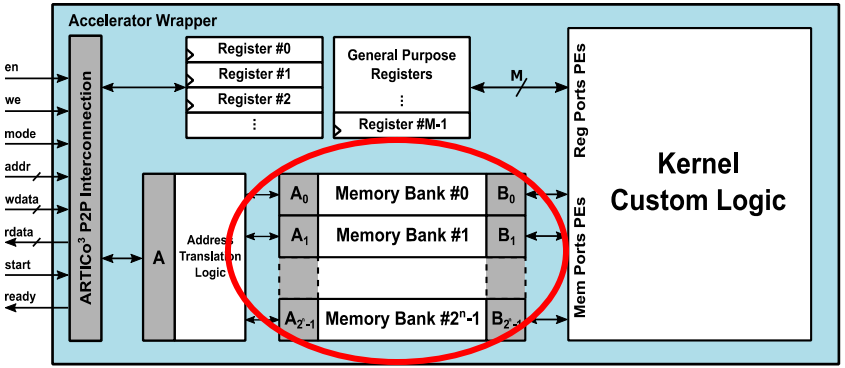

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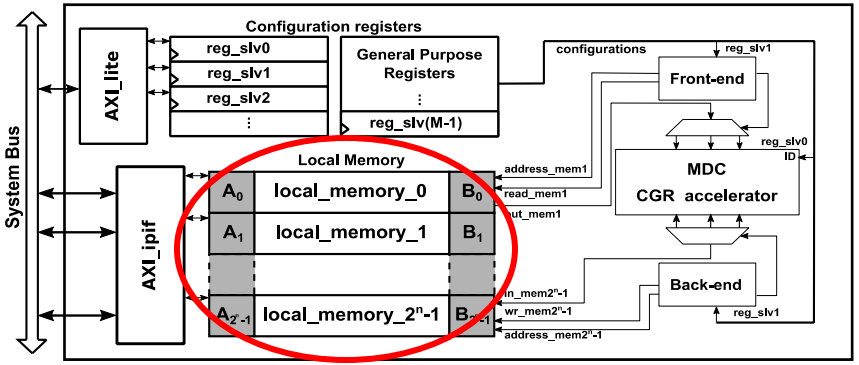

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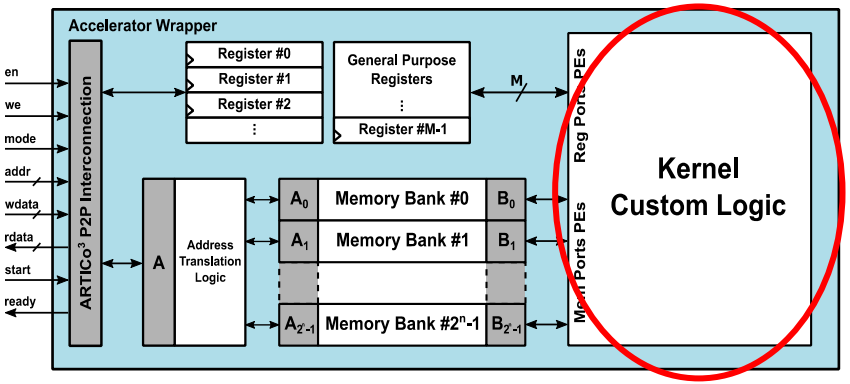

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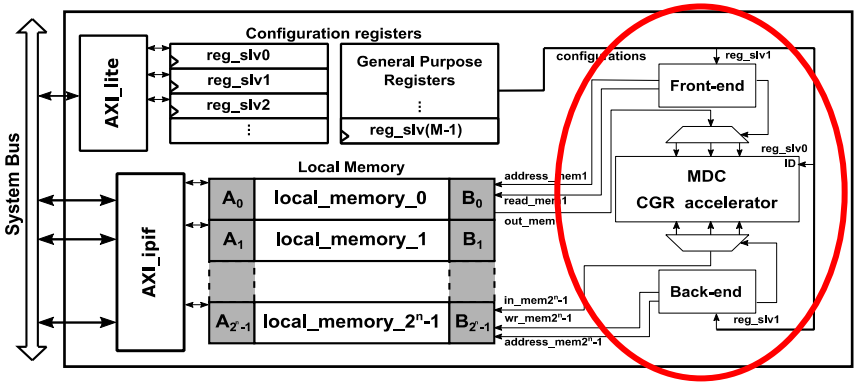

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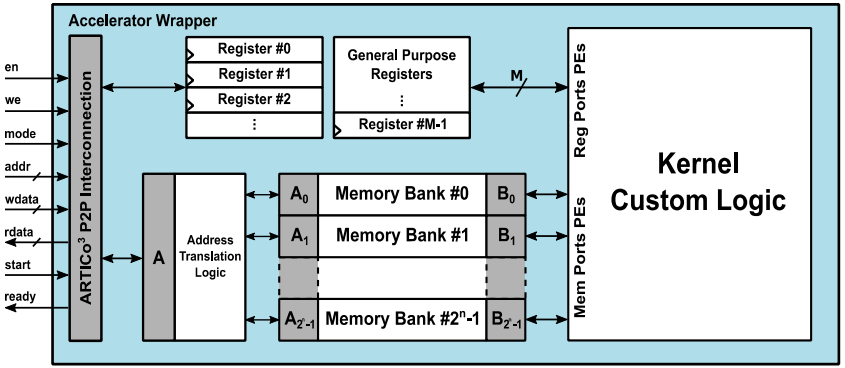

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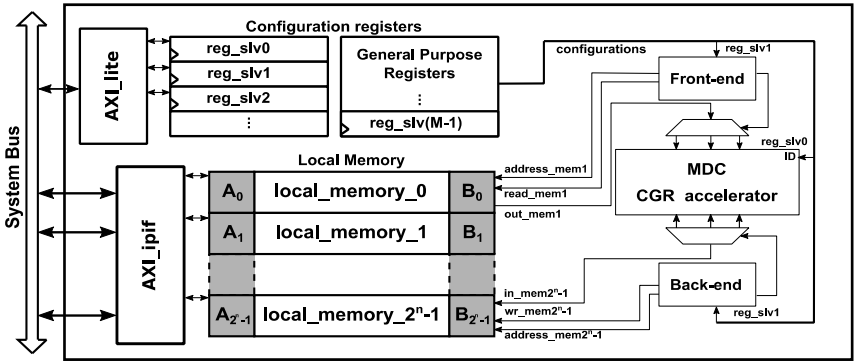

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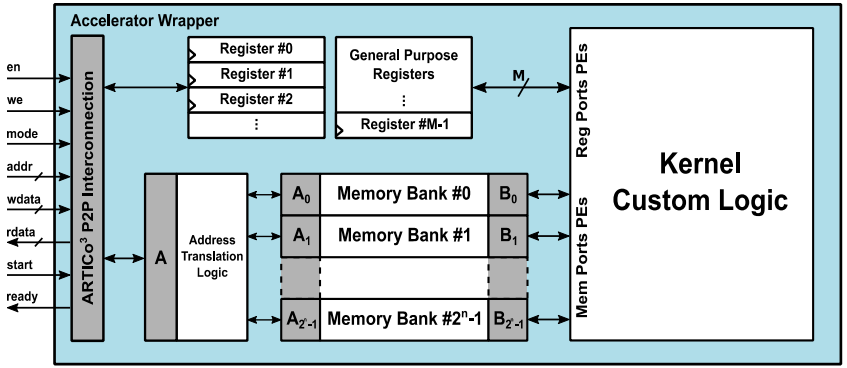

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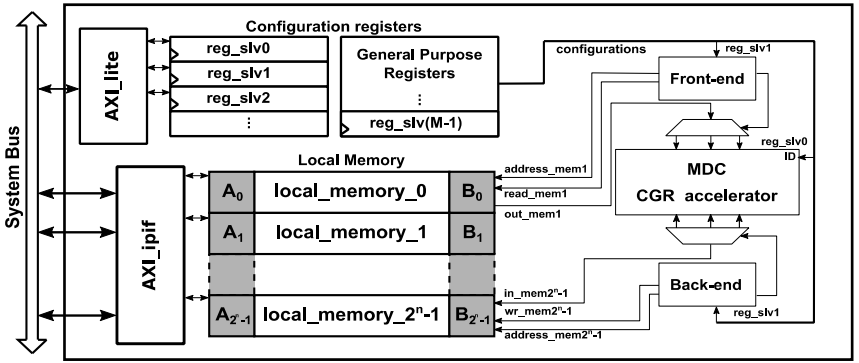
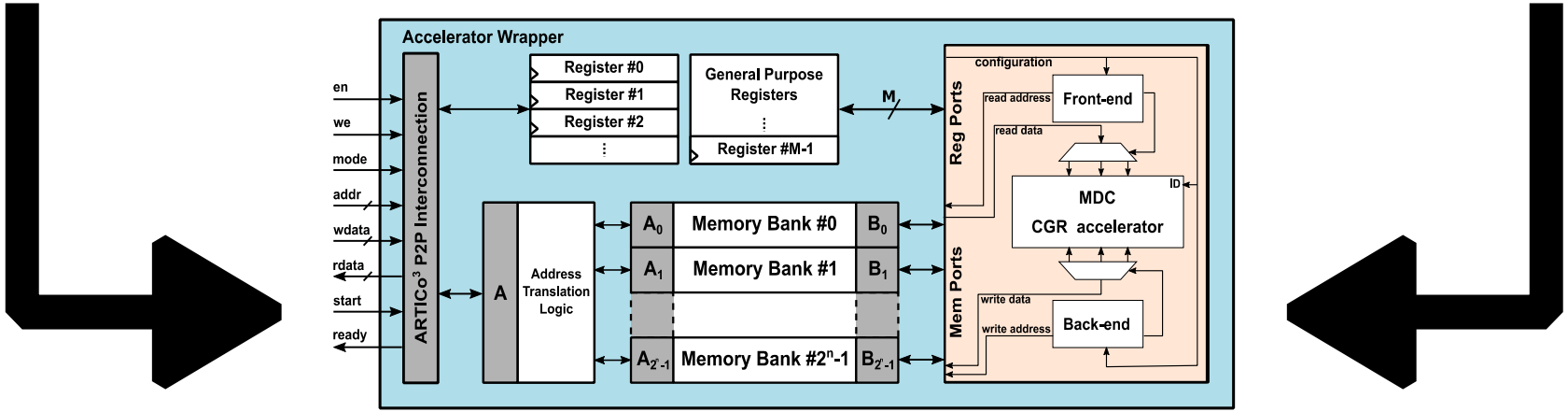
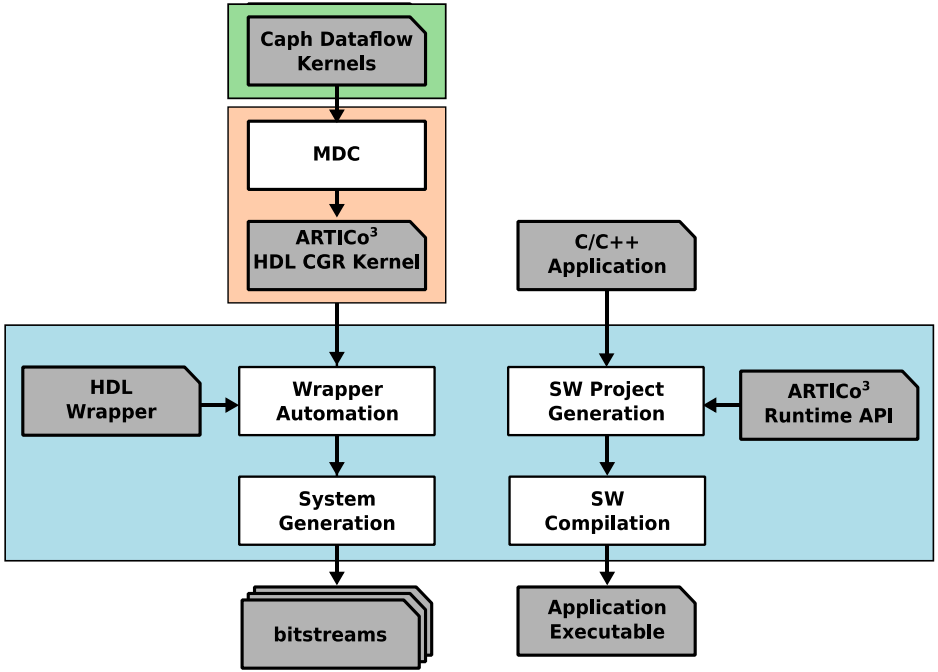




Multi-Grain Adaptivity



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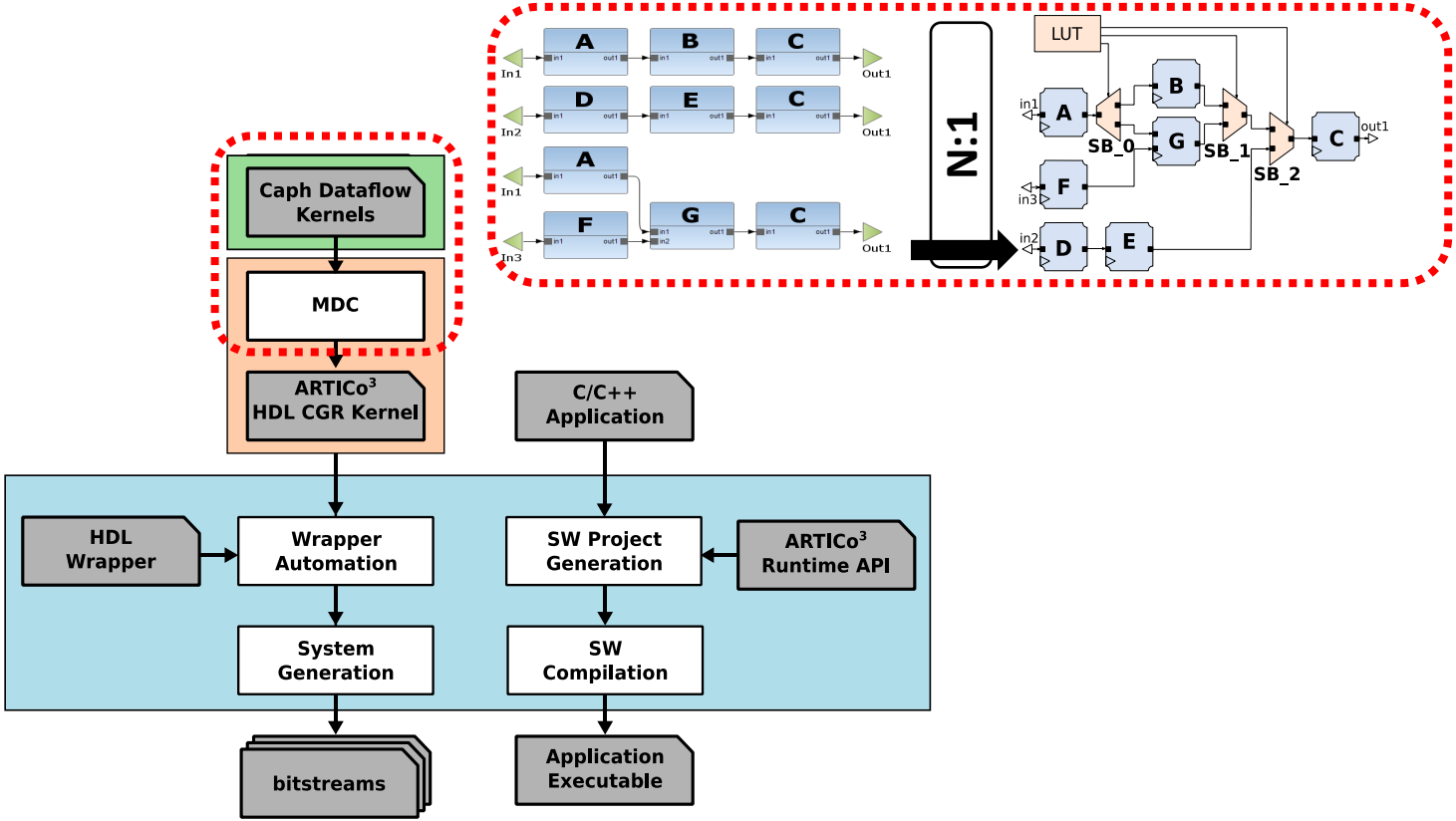

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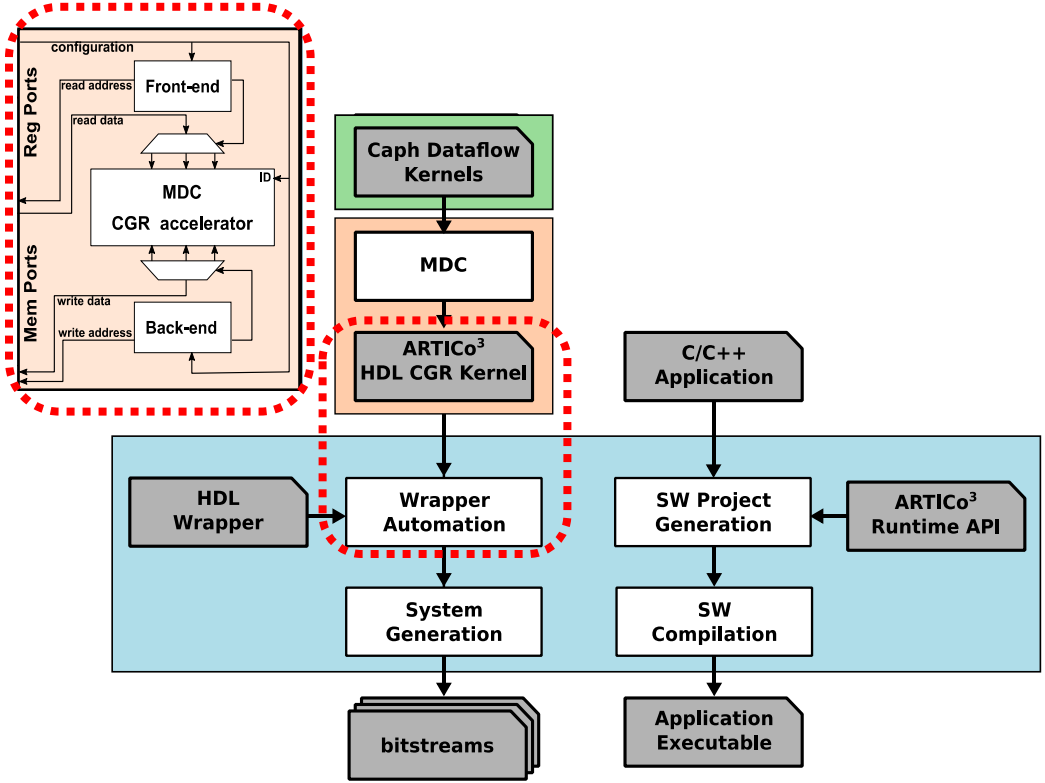

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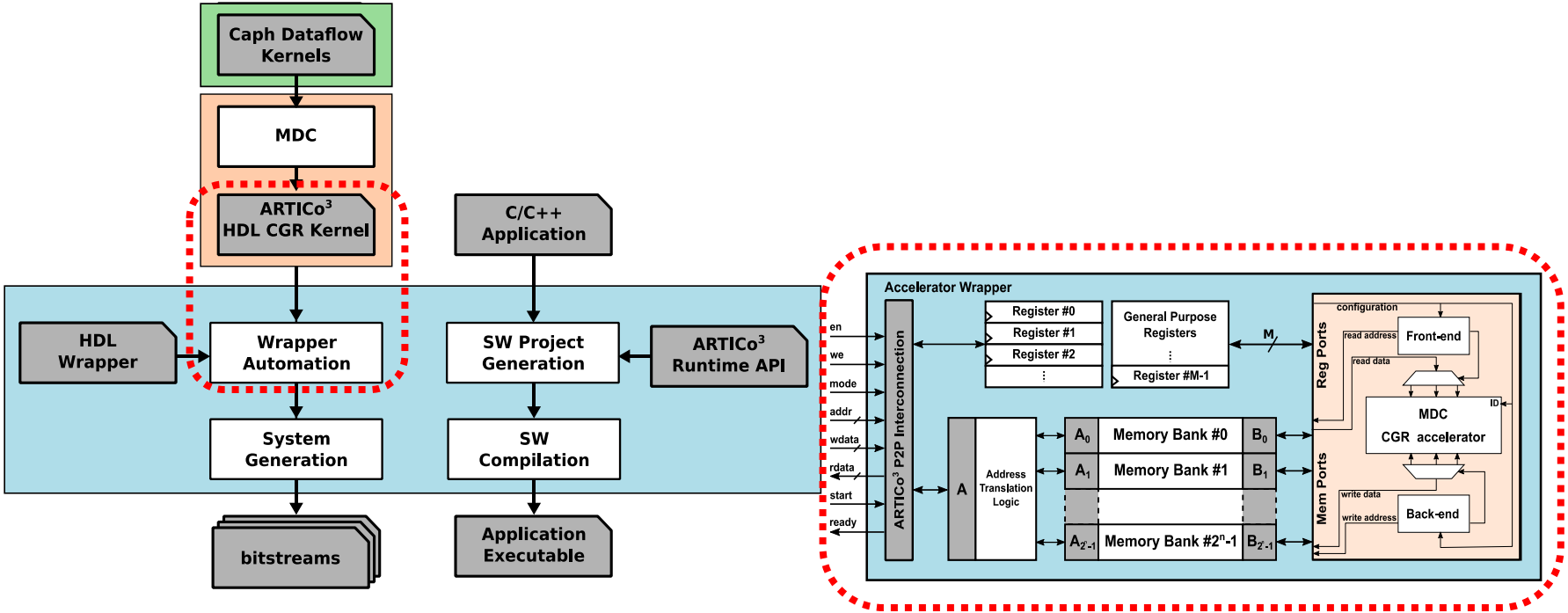

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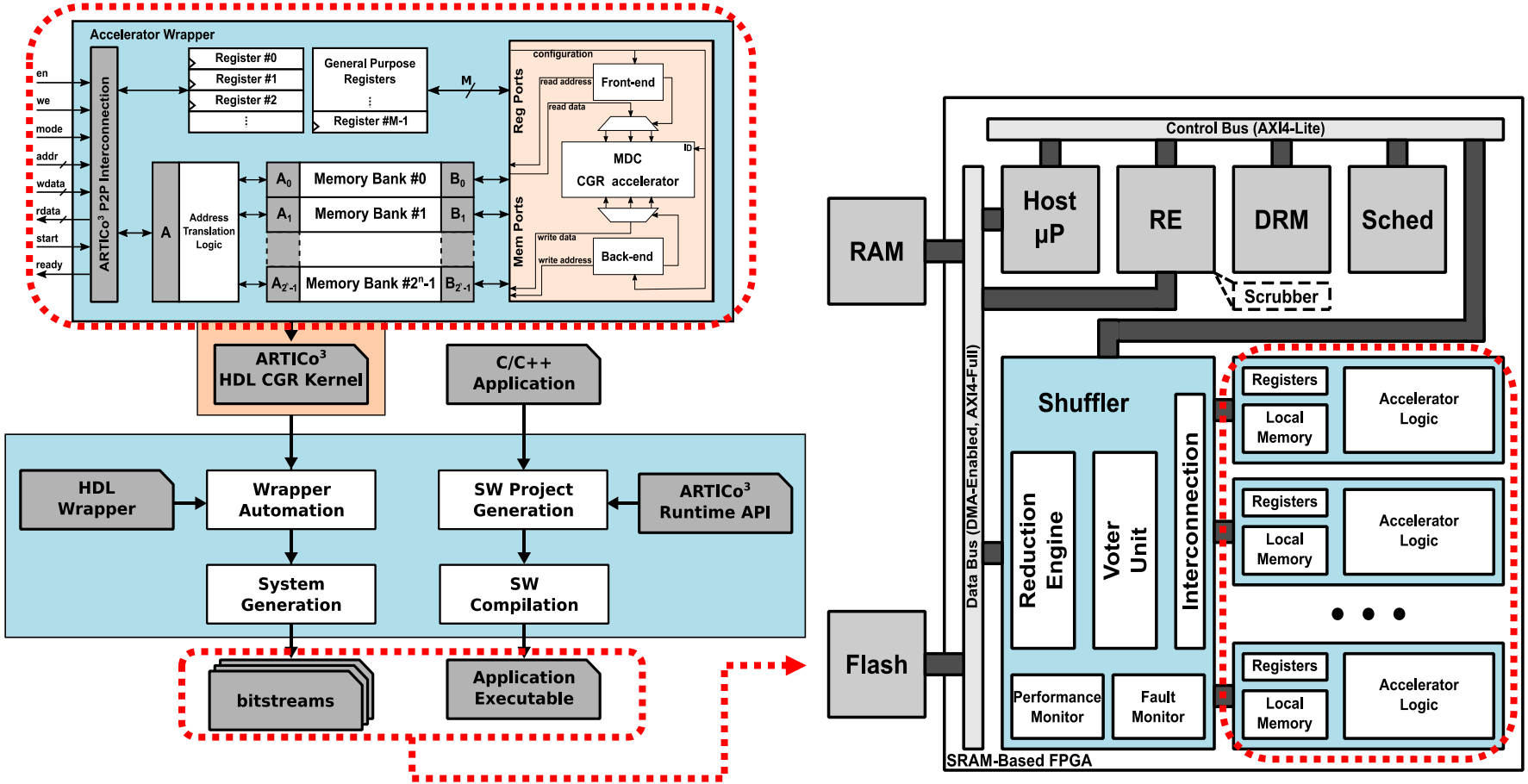

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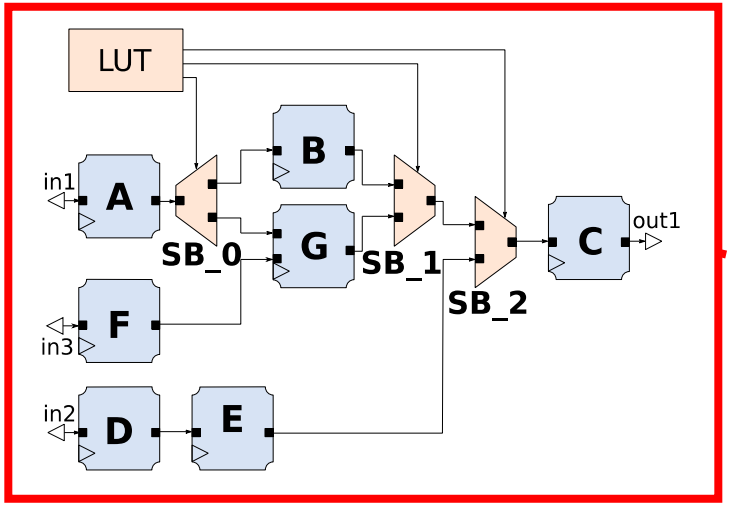

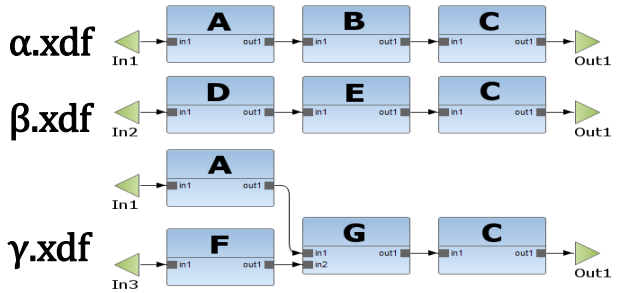

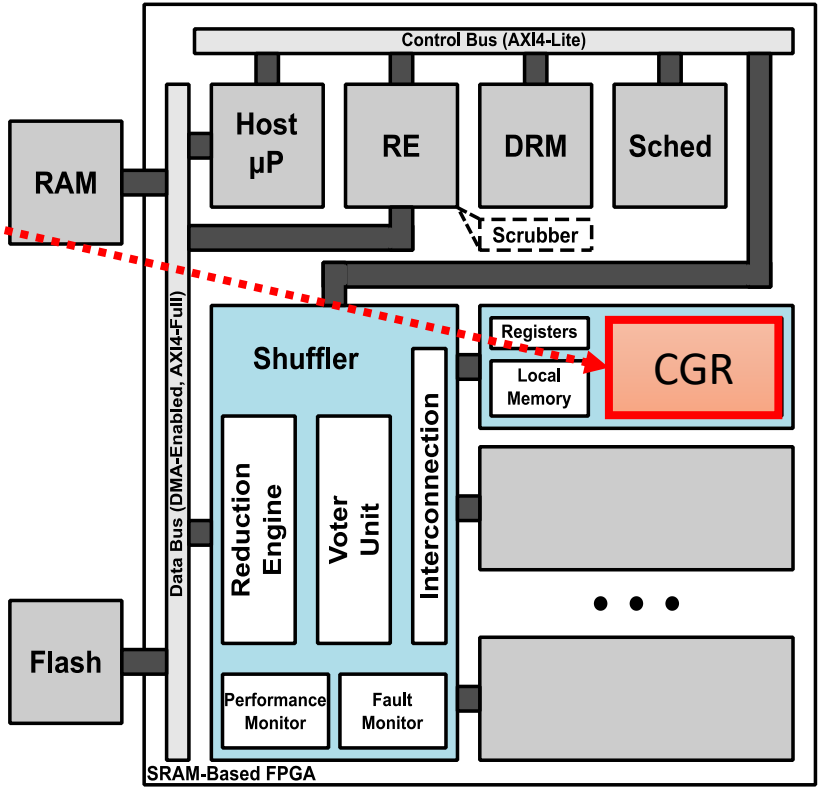

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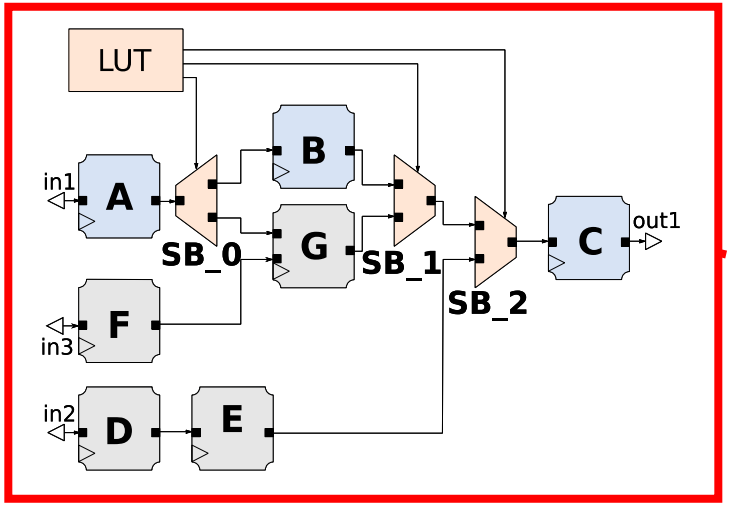

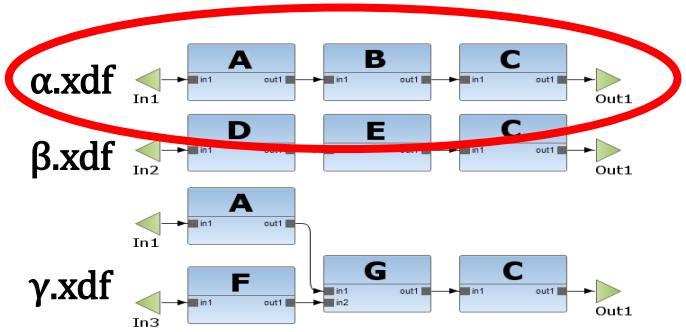

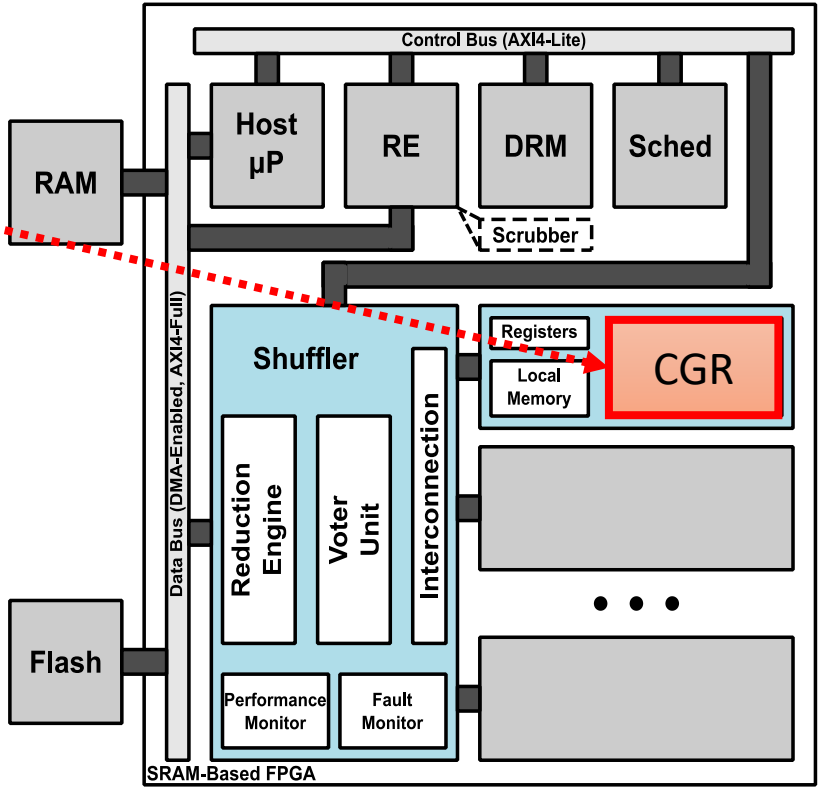

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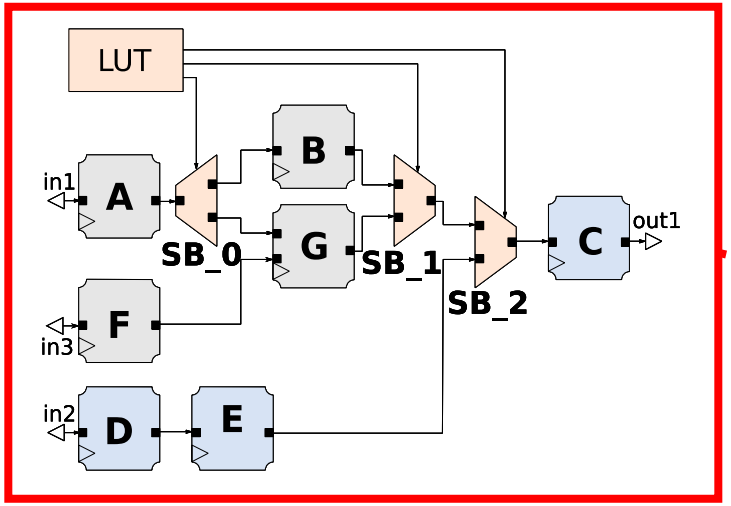

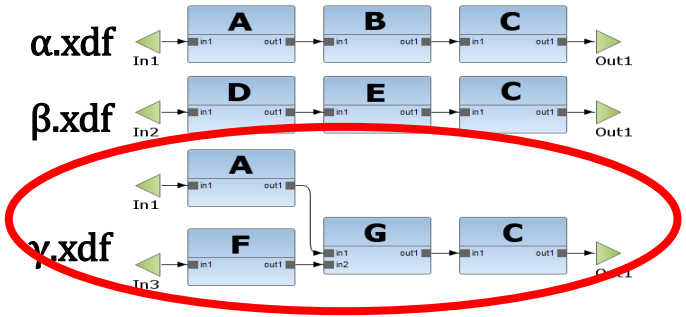

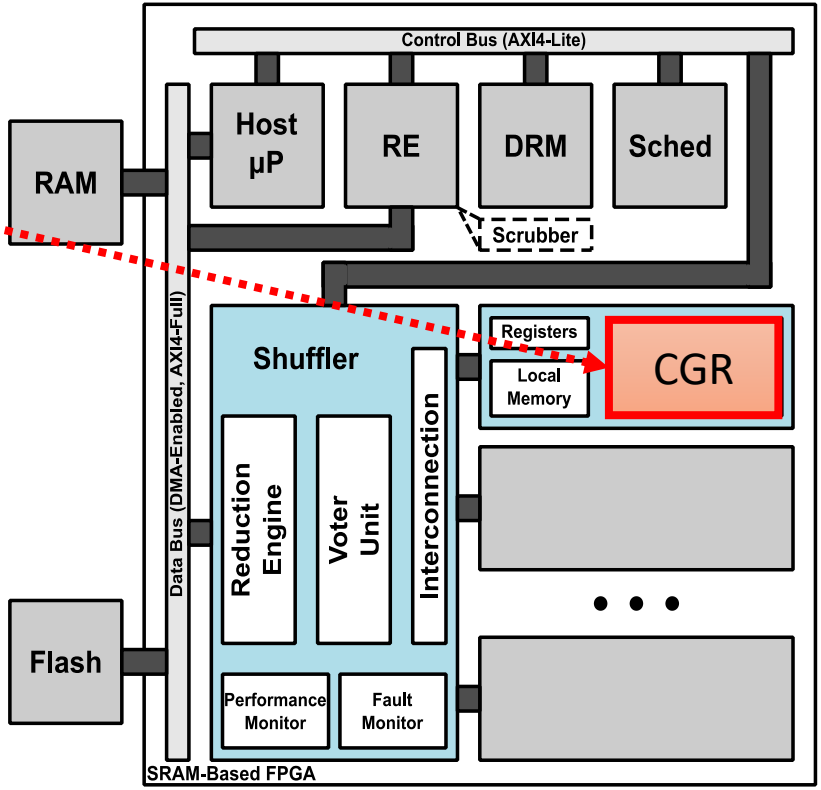

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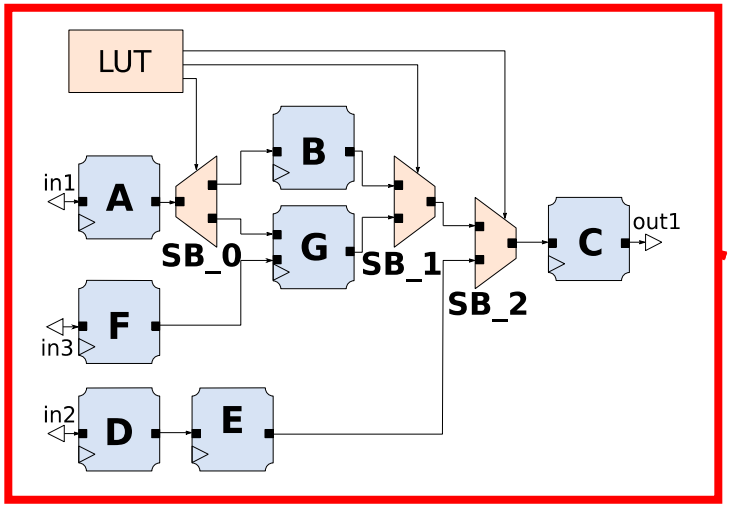

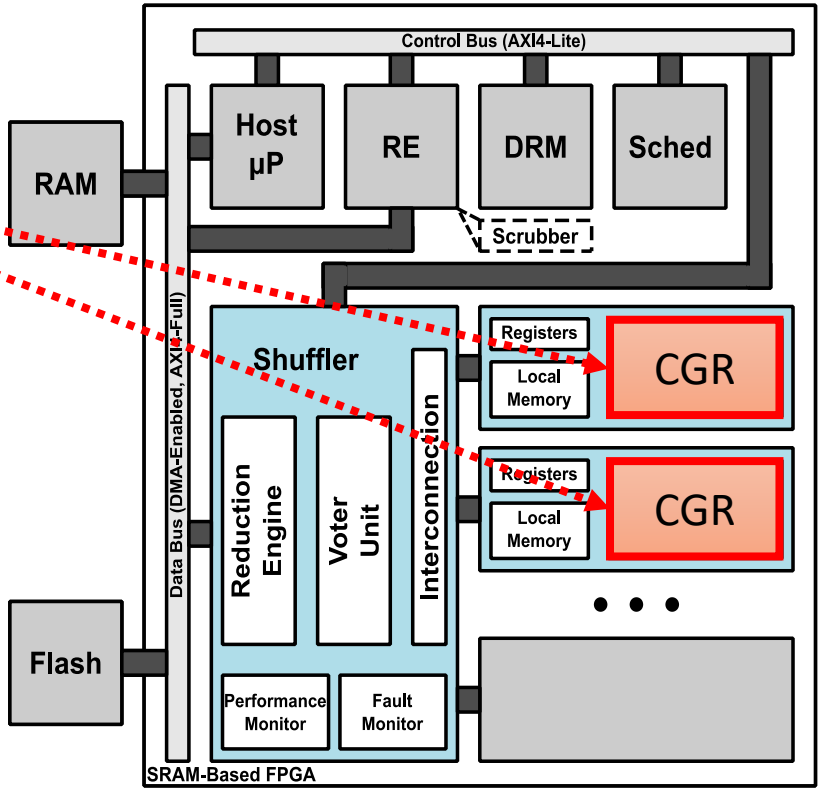

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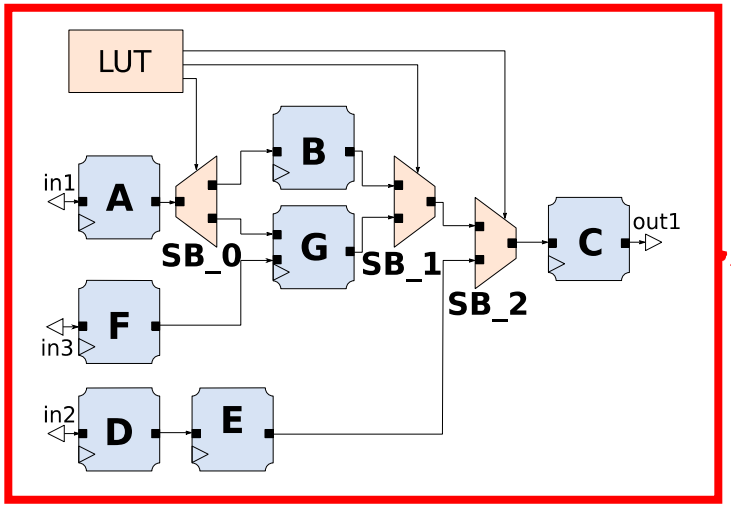

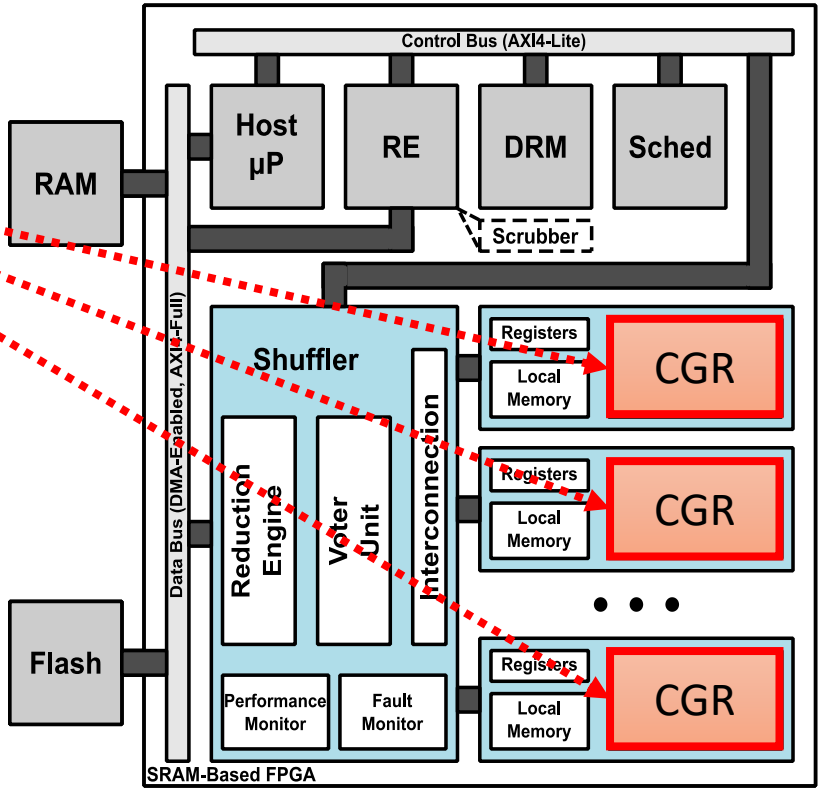

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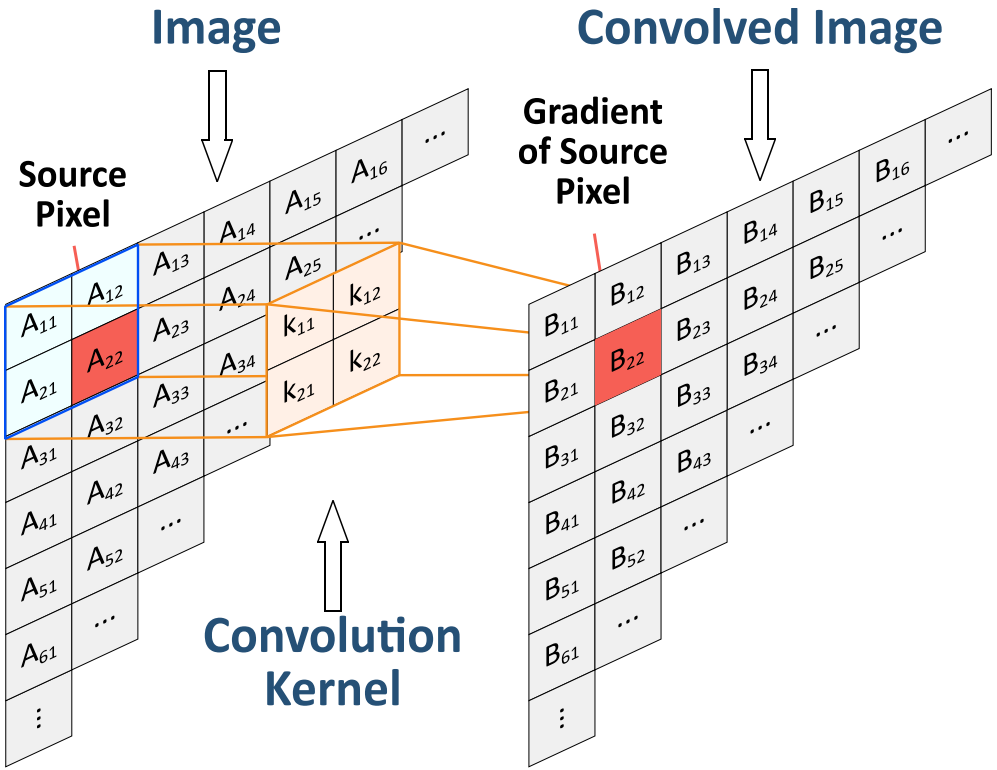

Roberts Operator

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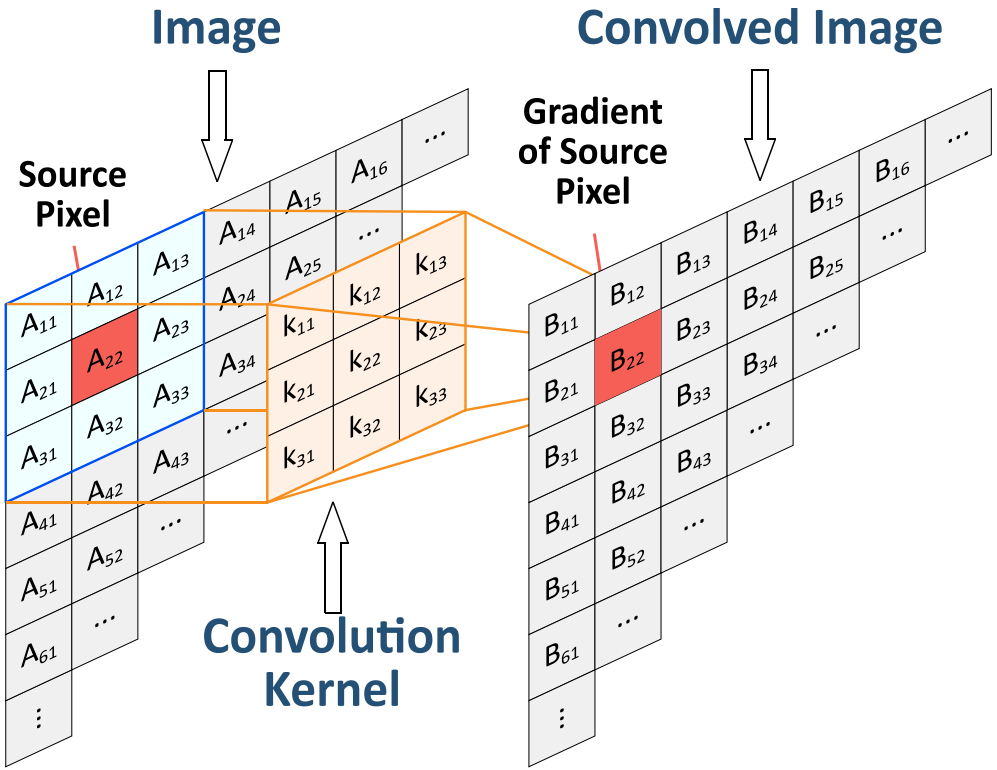

Sobel Operator

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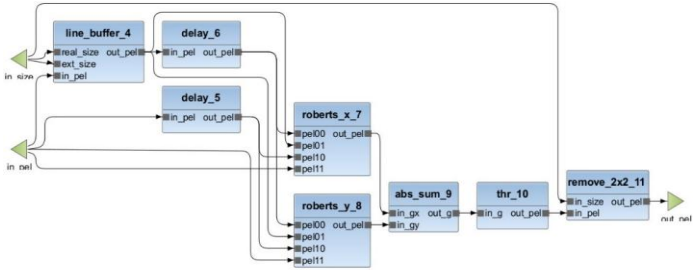

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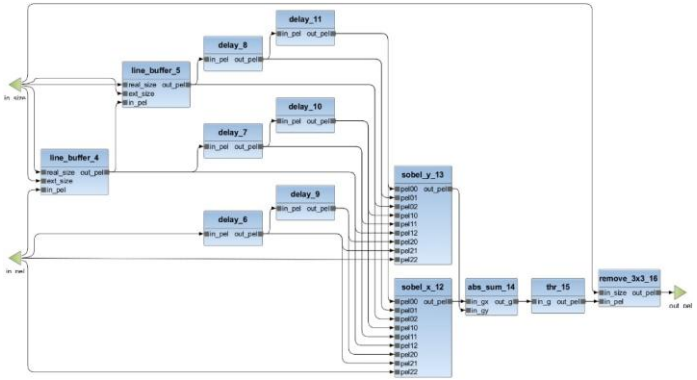

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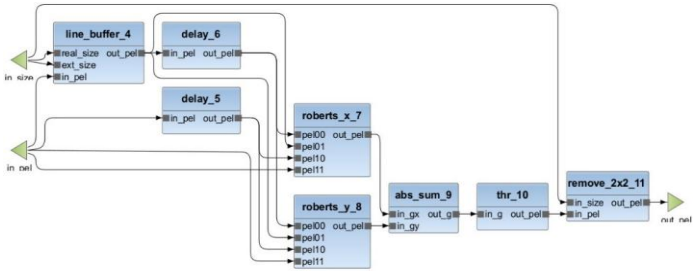

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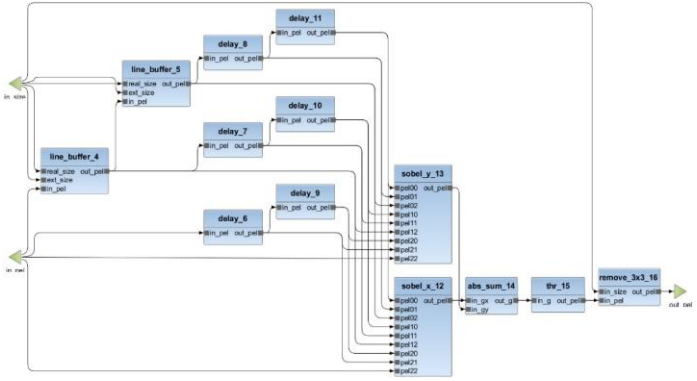
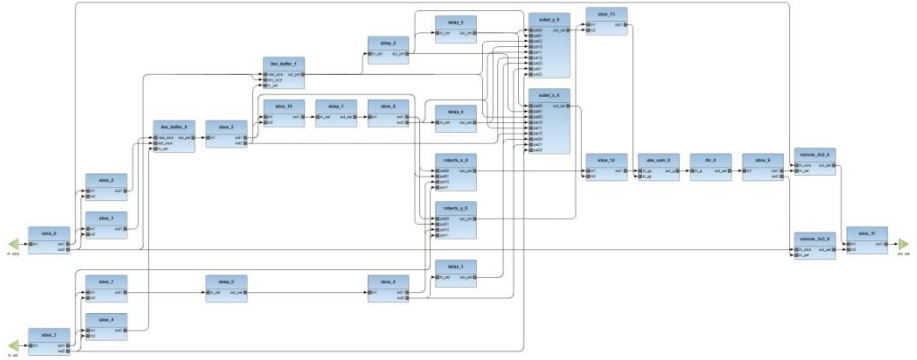


Coarse-Grain Reconfigurable (Sobel+Roberts)



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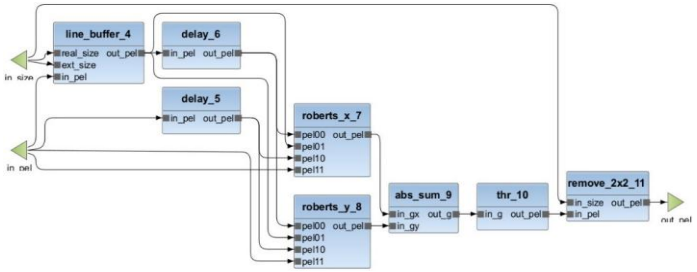

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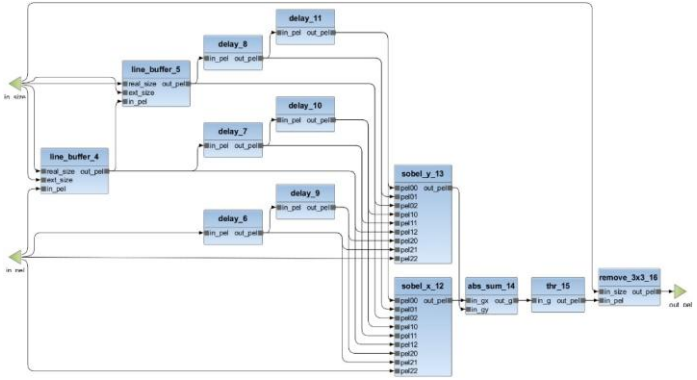

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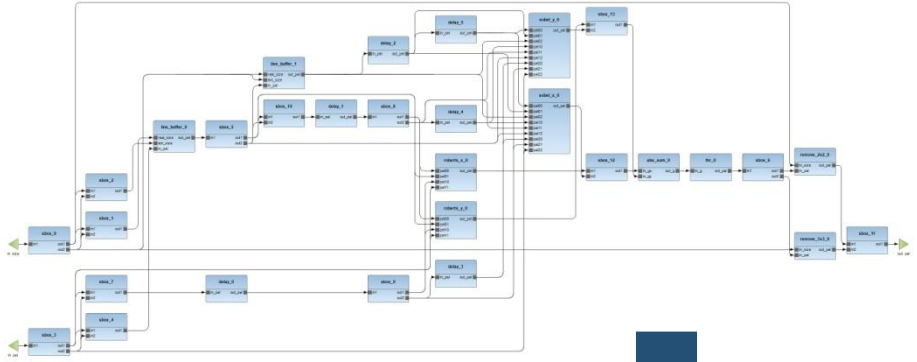

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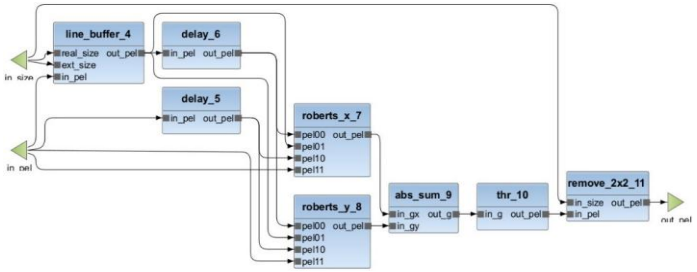

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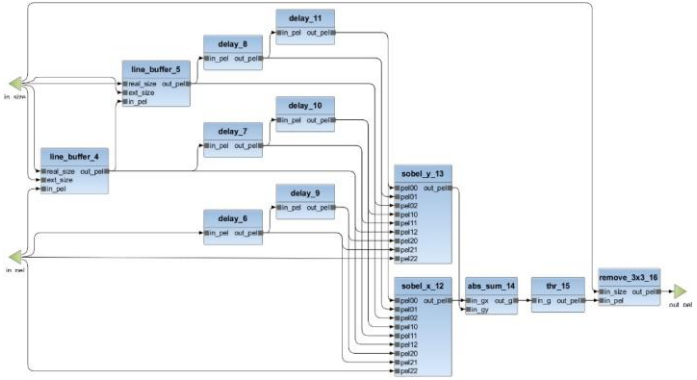

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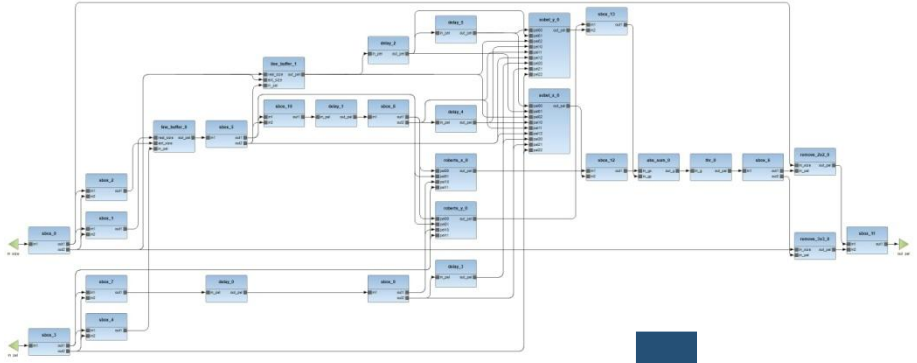
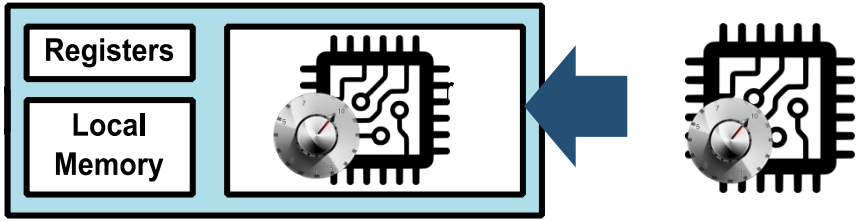


Tunable ARTICo^3 slot



Assessed Configurations

TARGET-DEVICE: *Custom Zynq-7000 board, based on the* ***XC7Z020CLG484-1*** *device, with* ***integrated power monitoring circuitry.***

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MULTI-GRAIN: heterogeneous reconfigurable MDC-generated *reconfigurable* kernels instantiated within the slots of the ARTICo3 architecture. The number of slots ranges from 1 to 4.

Experimental Results – Timing [fps]

	256x256	512x512	1024x1024	20148x20148
FG: 1 slot	29.95	6.61	1.65	0.42
FG: 2 slots	+ 24%	+26%	+28%	+25%
FG: 3 slots	+28%	+36%	+37%	+34%
FG: 4 slots	+37%	+ 44%	+44%	+40%
CG: 4 parallel	+37%	+44%	+45%	+42%

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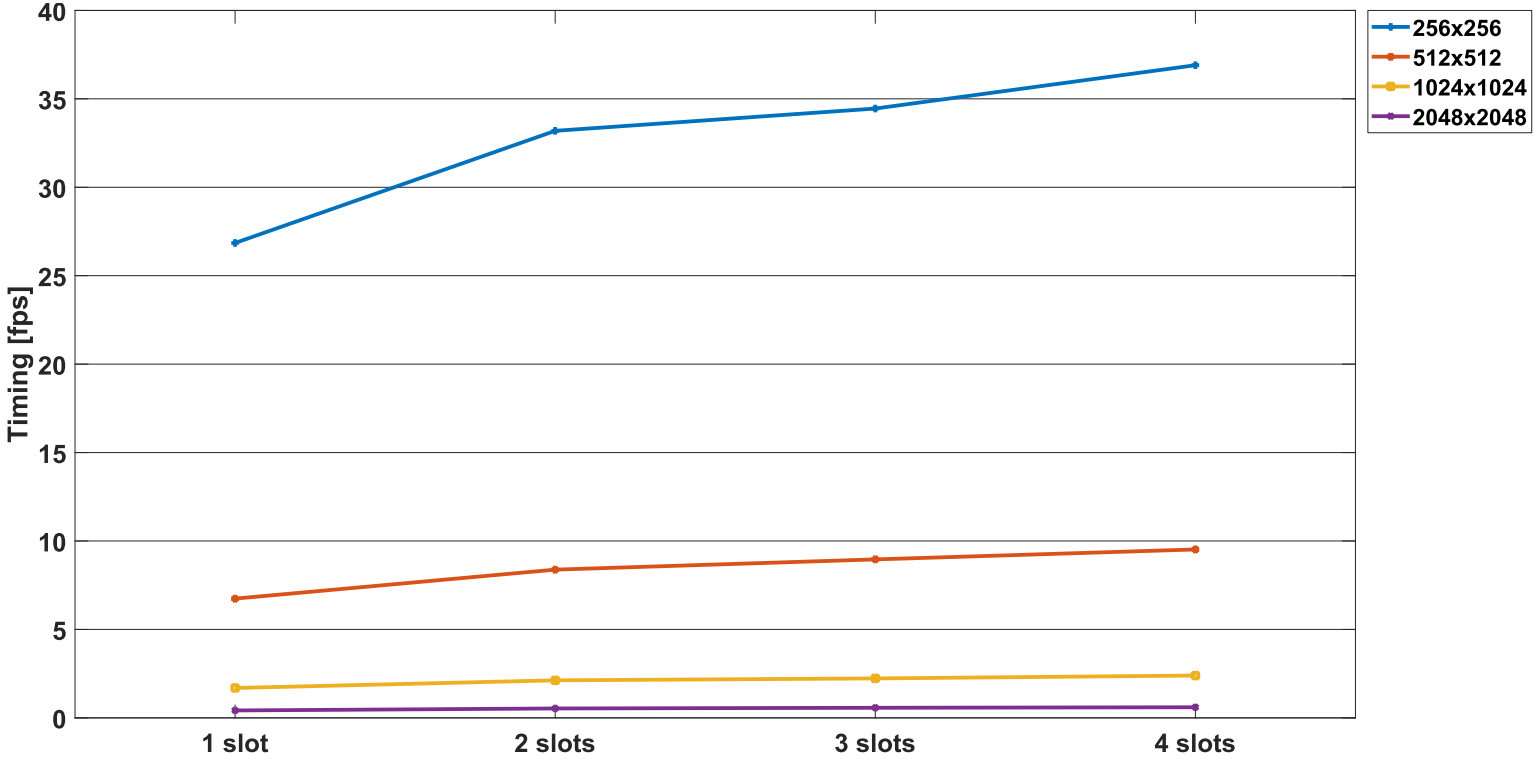
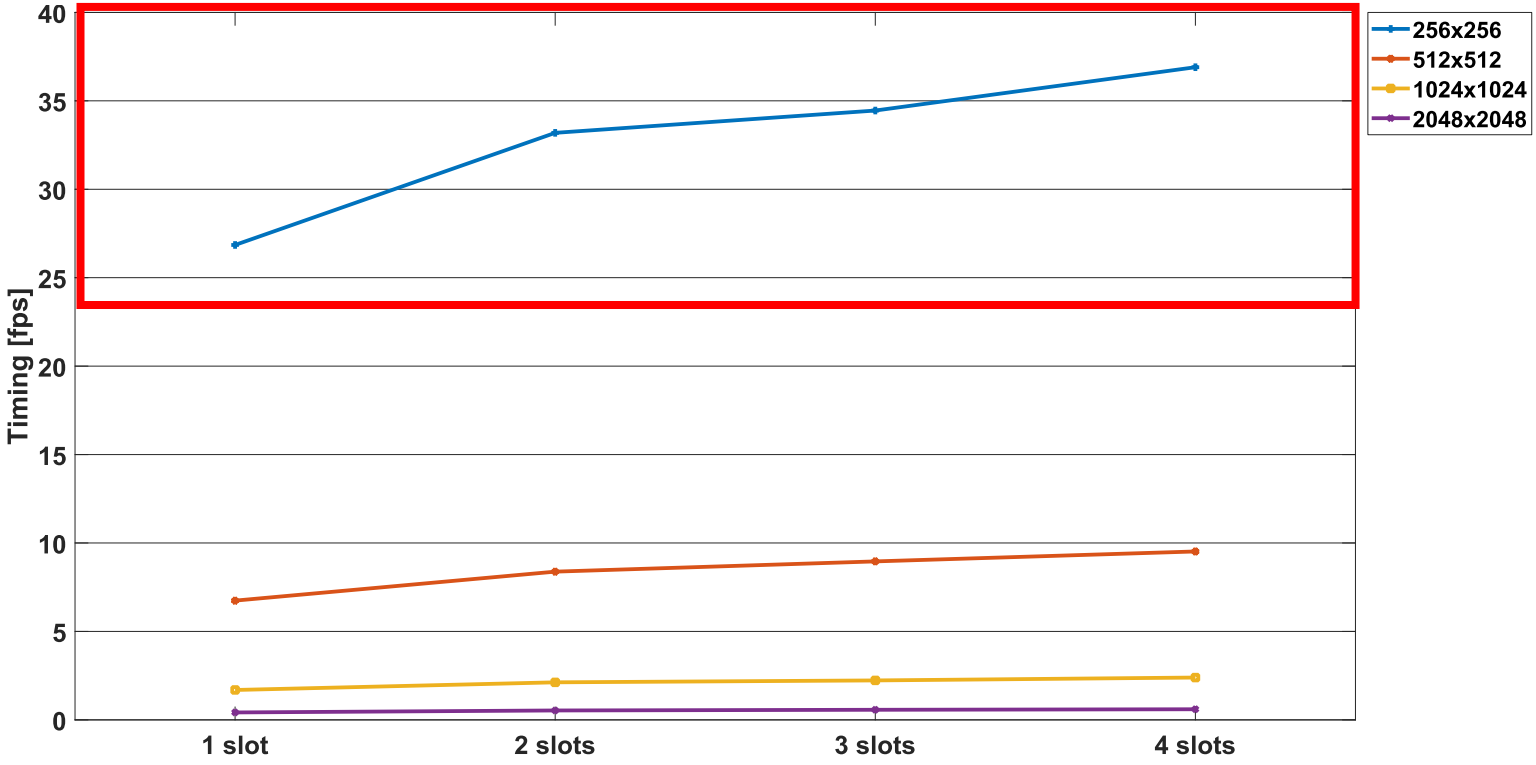
Experimental Results – Timing [fps]

MULTI-GRAIN



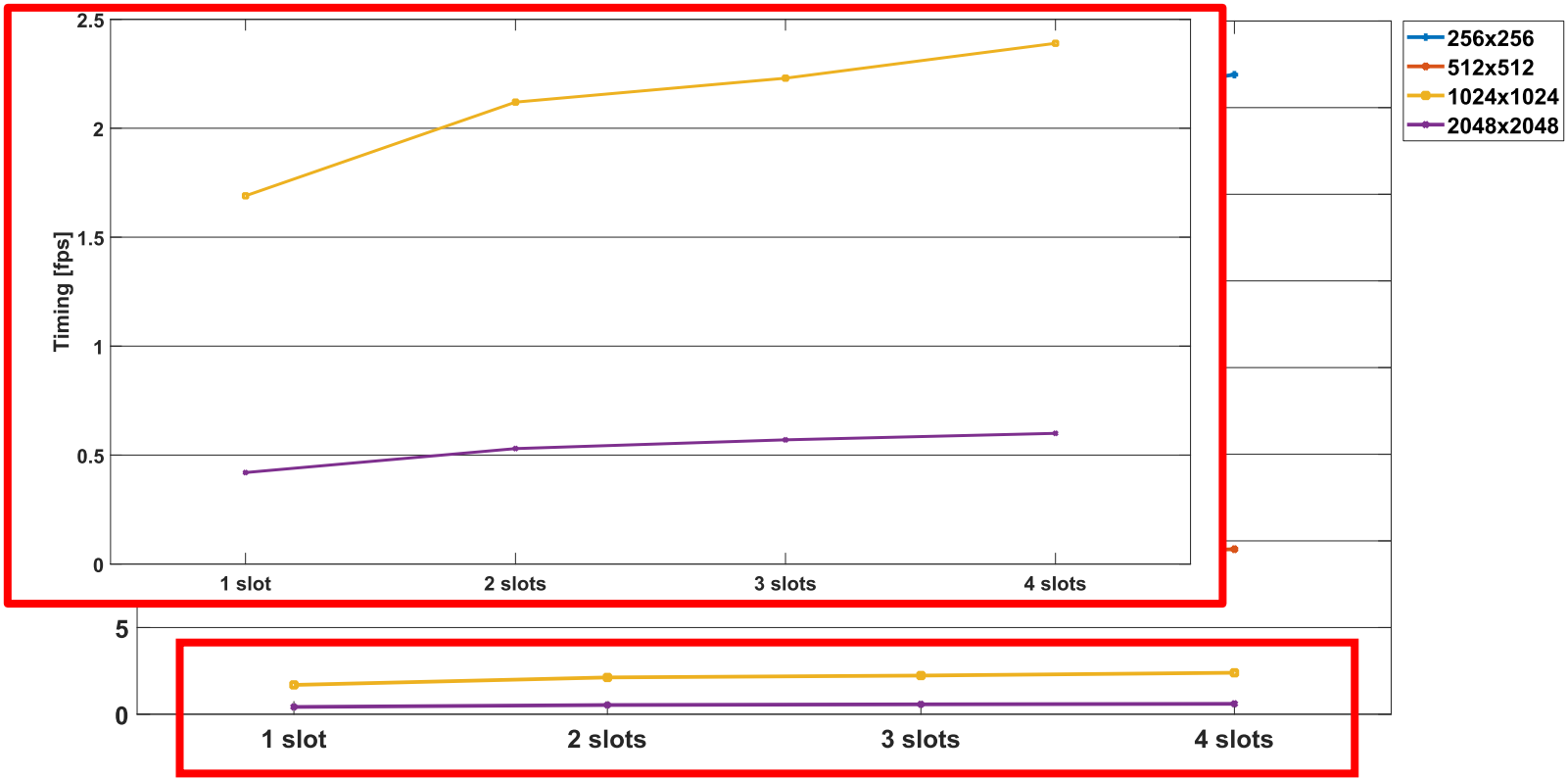
Experimental Results – Timing [fps]

MULTI-GRAIN



Experimental Results – Timing [fps]

MULTI-GRAIN



Experimental Results – Energy [mJ]

	256x256	512x512	1024x1024	20148x20148
FG: 1 slot	33.47	130.32	532.13	2132.95
FG: 2 slots	-14%	-17%	-17%	-17%
FG: 3 slots	-20%	-21%	-23%	-23%
FG: 4 slots	-24%	-24%	-25%	-26%
CG: 4 parallel	-15%	-25%	-25%	-26%

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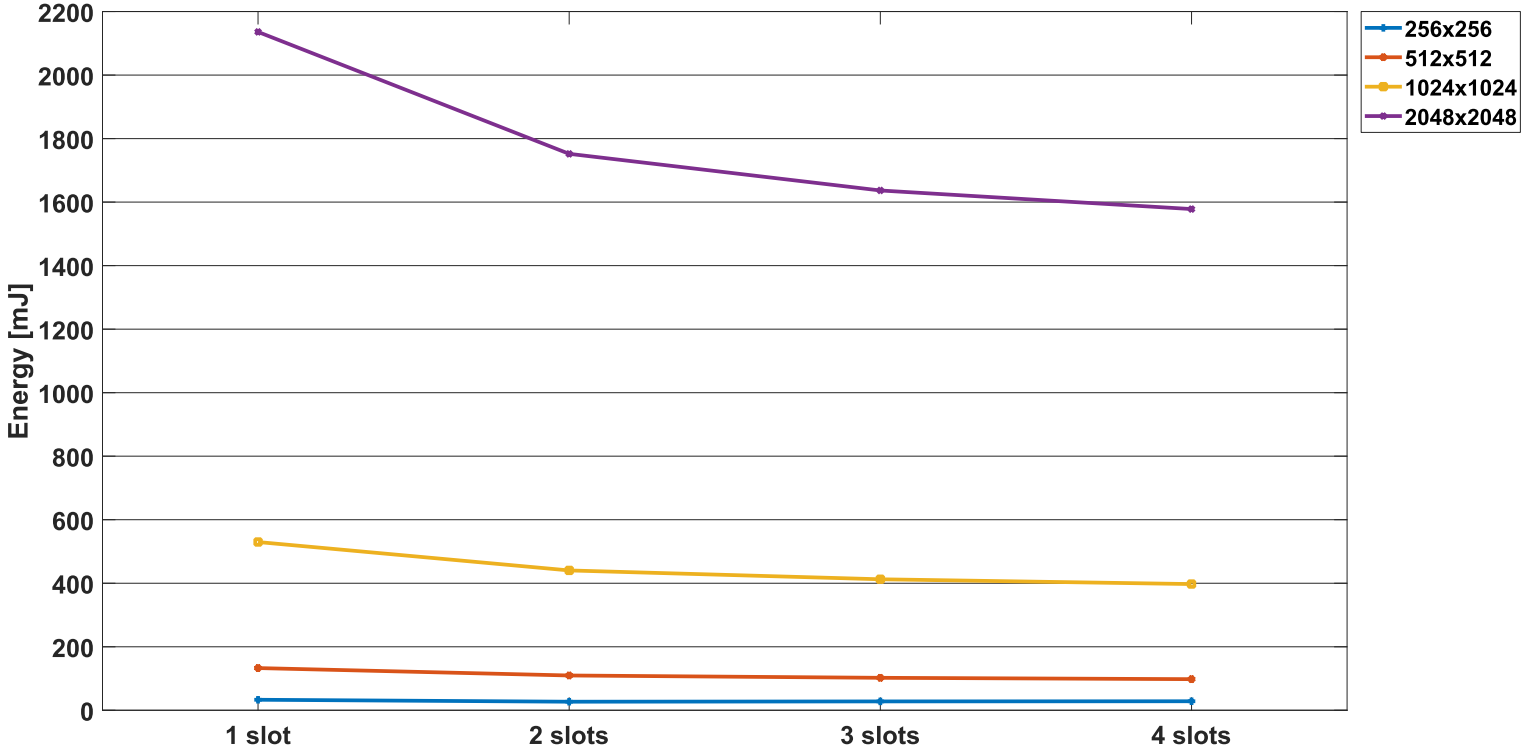

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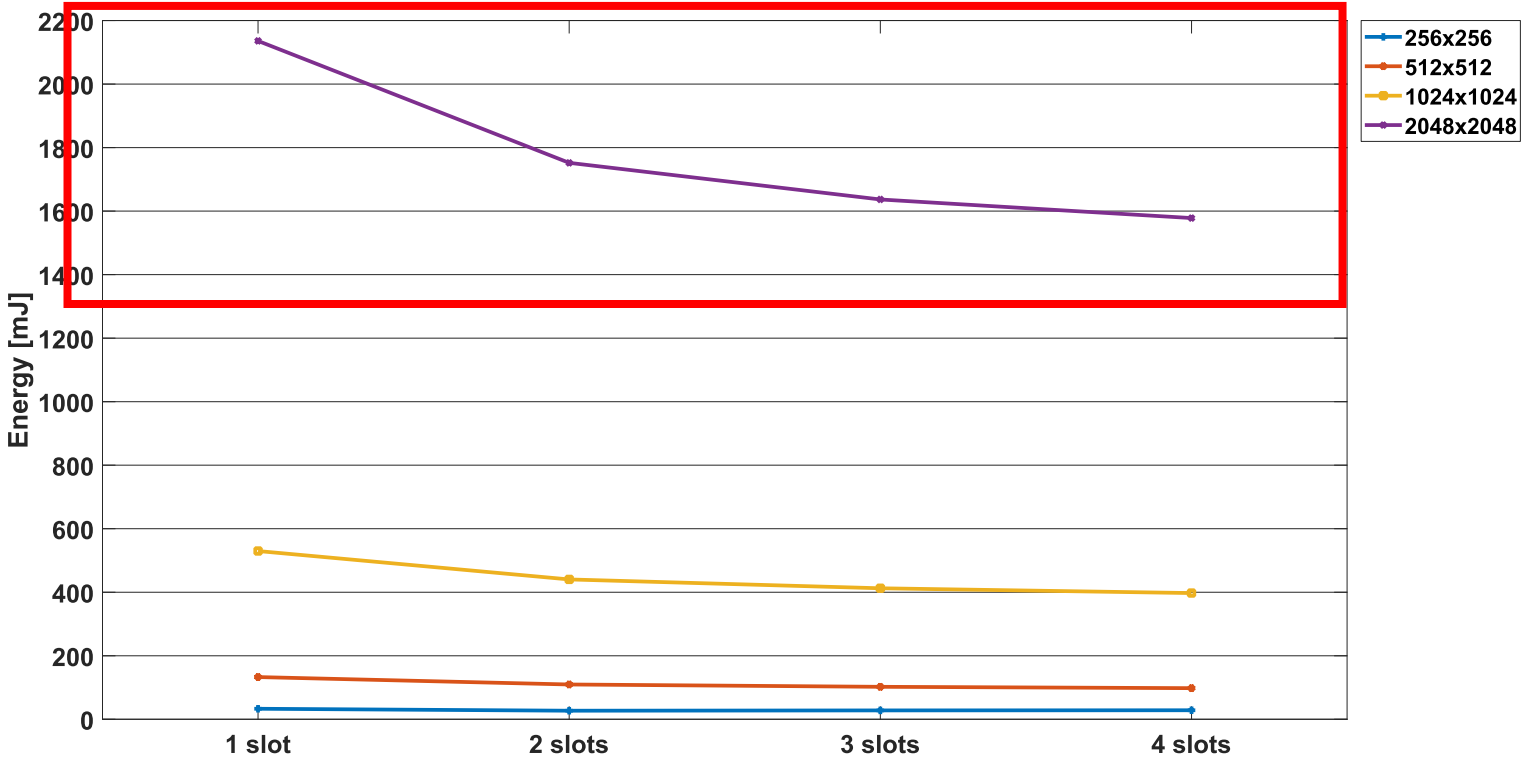
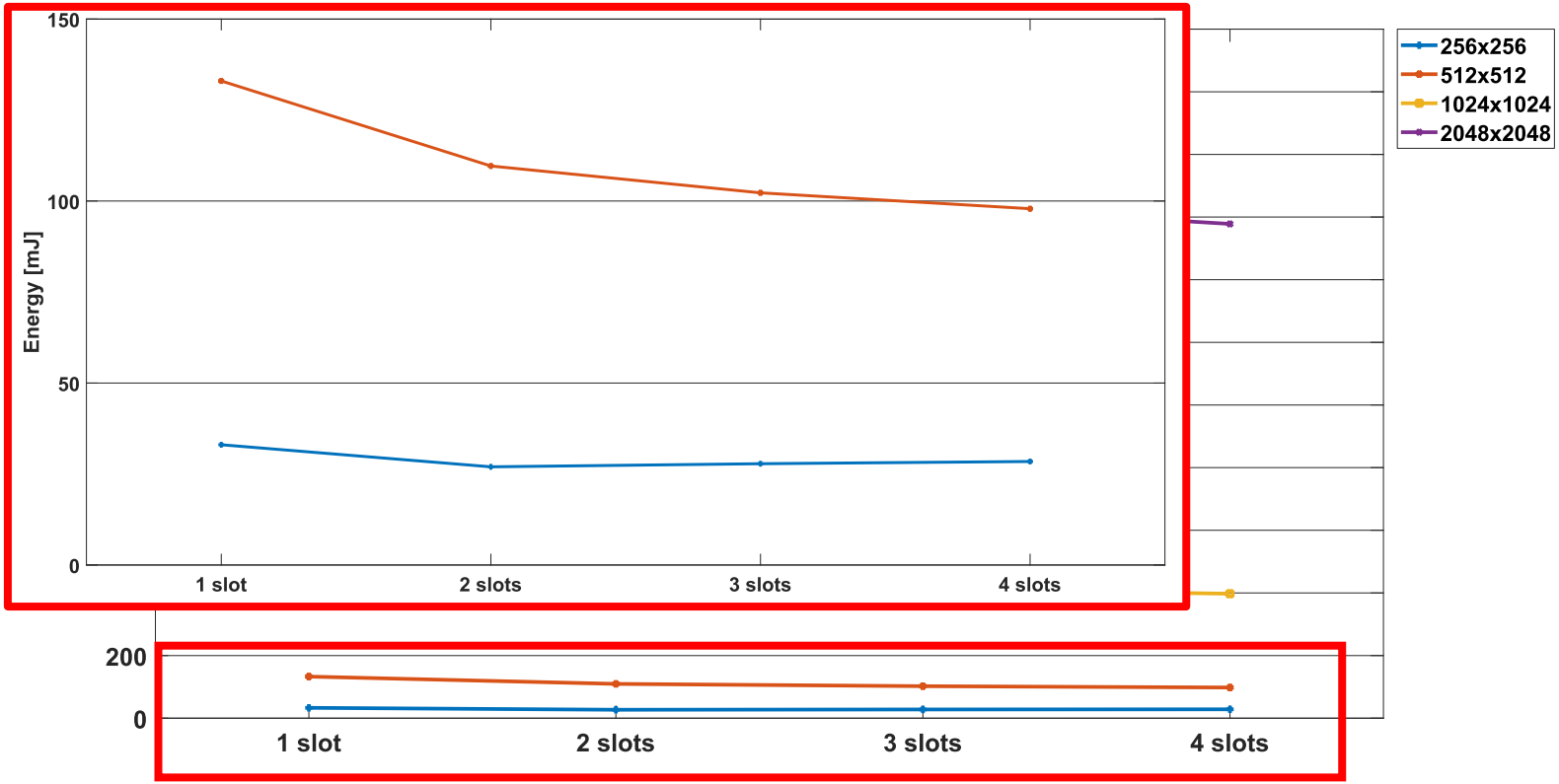
MULTI-GRAIN



Experimental Results – Energy [mJ]

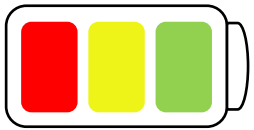
MULTI-GRAIN



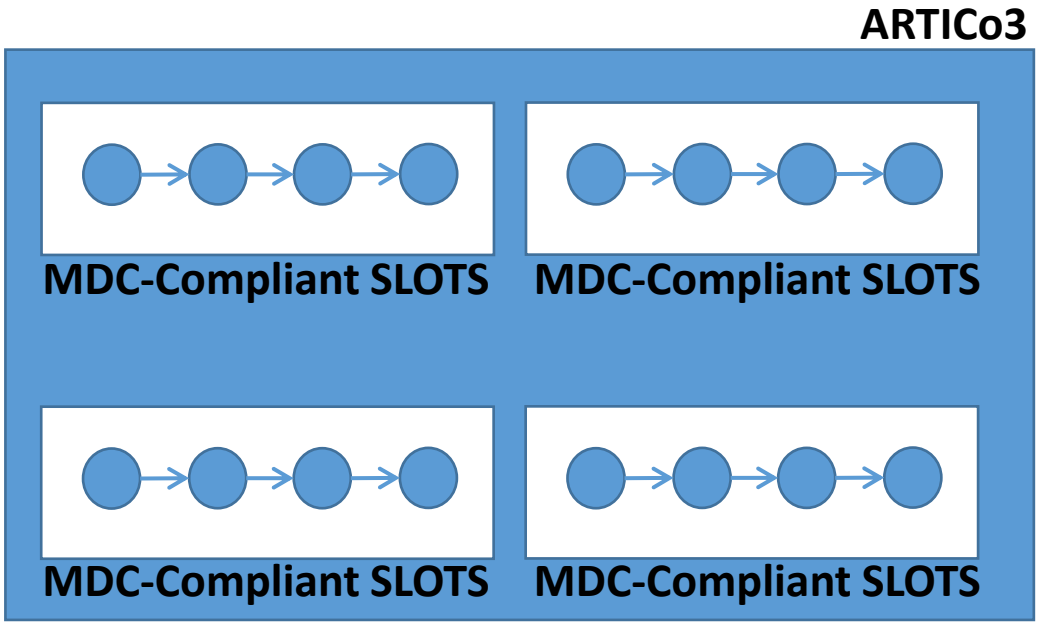
Experimental Results – Reconfiguration Overhead

	Size [B]	Time [ms]	Energy [mJ]
FG: 1 slot	858k	16.42	15.18
FG: 2 slots	1715k	47.62	51.91
FG: 3 slots	2573k	75.95	67.1
FG: 4 slots	3430k	106.14	94.11
CG: 4 parallel	2	0.09	0.11

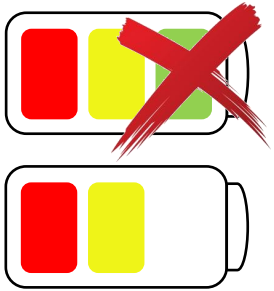
Mixed-Grain: The Best of Both



Max Troughput
Max QoS

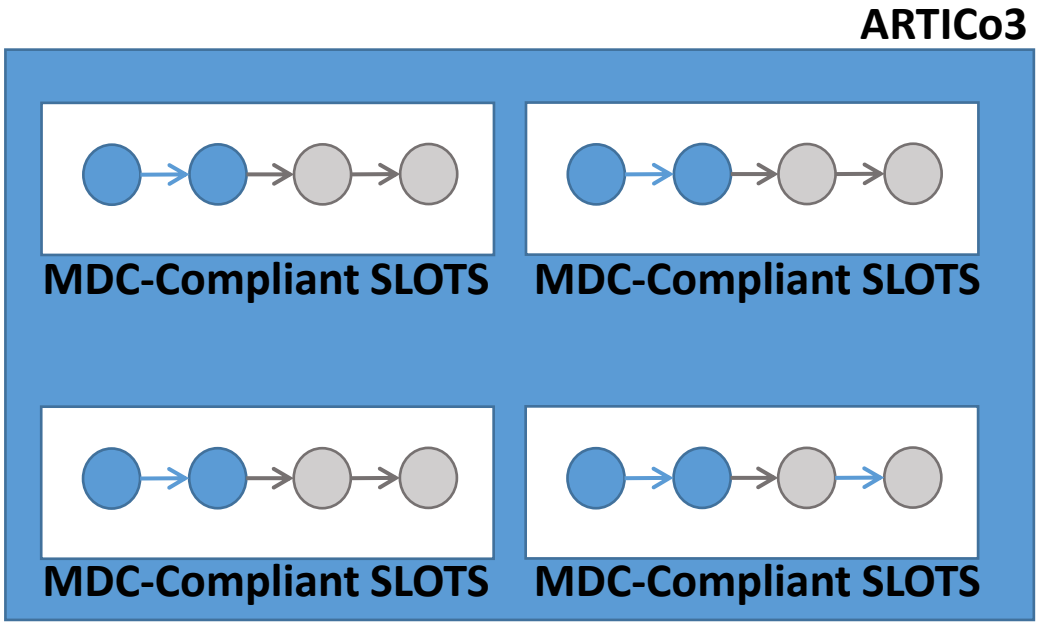


Mixed-Grain: The Best of Both

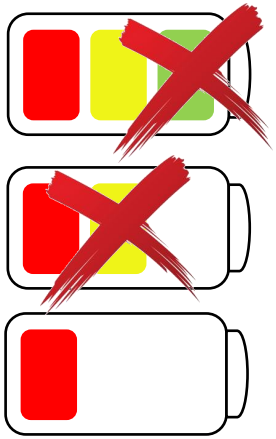


Max Troughput
Max QoS

Max Troughput
Degraded QoS



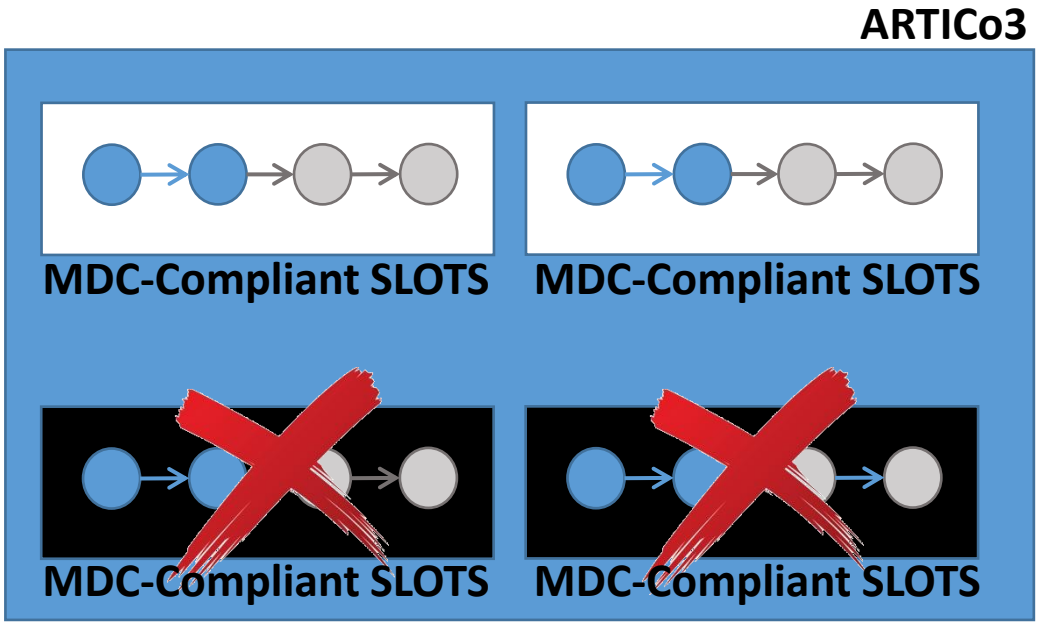
Mixed-Grain: The Best of Both



Max Troughput
Max QoS

Max Troughput
Degraded QoS

Less Troughput
Degraded QoS



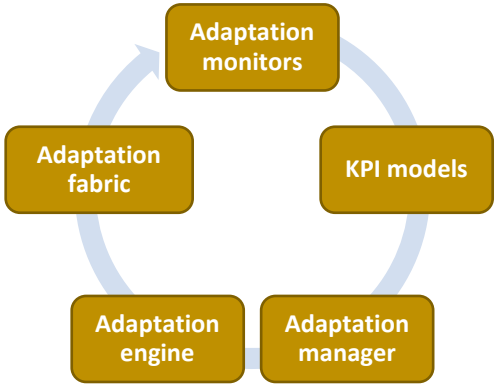
Conclusions

The presented toolchain integrates the **MDC** tool with the **ARTICo^3** framework, supporting the automatic development, from specification down to implementation, of **multi-grain reconfigurable systems**, speeding up the design process and facilitating their deployment and runtime management.

Experimental results of this proof-of-concept edge-detection test case demonstrated the potential of the approach in terms of **FPGA resources**, **timing** and **energy efficiency**.

The proposed methodology can be particularly useful in **CPS contexts**, where variability is common due to the involvement of **user**, **environment** or **system requirements**.

Future Works



PAPI (UPM-CITSEM)

MONITOR

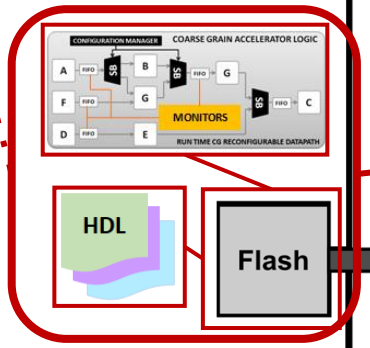
ACT – RECONFIGURE - ACT

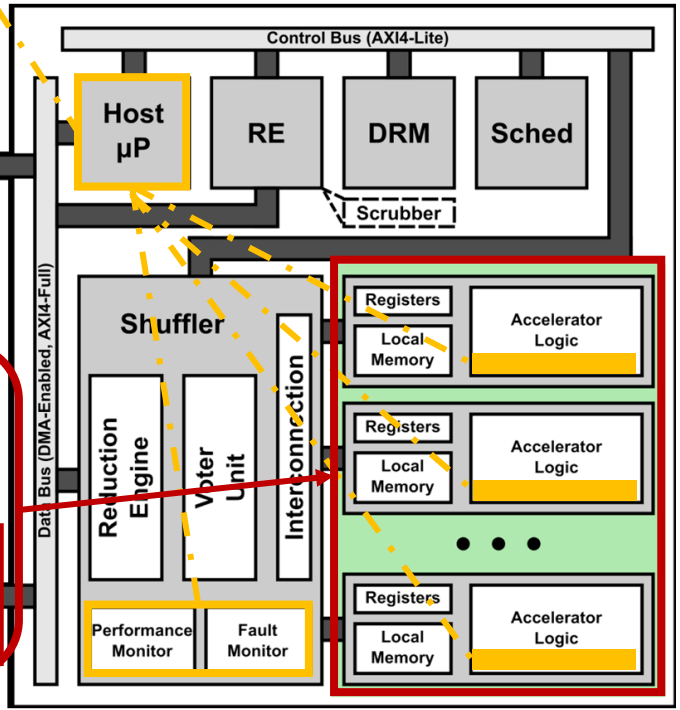
INFORM

SPIDER (INSA-RENNES)

DECIDE

Bitstreams





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Siena, 13-14 September 2018

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Thank you for your attention

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