

ENFORCING CONTROL-FLOW INTEGRITY IN VIRTUALIZED ENVIRONMENTS ON ARM PLATFORMS

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MOTIVATION AND CONTEXT

**Can we really trust our embedded devices?
Imagine if this will happen on our cars or trains.**

iOS 14.4 and iPadOS 14.4

Released January 26, 2021

WebKit

Available for: iPhone 6s and later, iPad Air 2 and later, iPad mini 4 and later, and iPod touch (7th generation)

Impact: **A remote attacker may be able to cause arbitrary code execution.** Apple is aware of a report that this issue may have been actively exploited.

Description: A logic issue was addressed with improved restrictions.

CVE-2021-1871: an anonymous researcher

CVE-2021-1870: an anonymous researcher



Embedded systems

- OSes are written in C/C++
- Exposed to public access



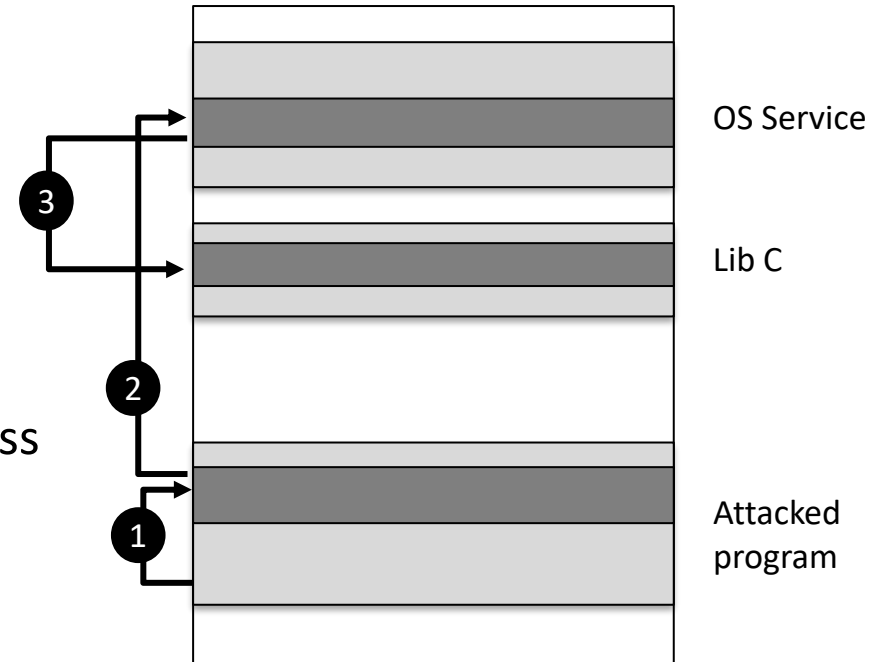
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Susceptible to attacks

- **Code-Reuse-Attacks**
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 - I.e. flow deviated to gain root access
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Mitigation technique

- Address space layout randomization (ASLR)
- **Integrity check of control flow (CFI)**



INTRODUCTION

CFI basic idea:

- build a Control Flow Graph (CFG) of the program
- **CFG** defines the legal execution

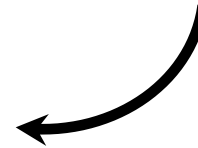
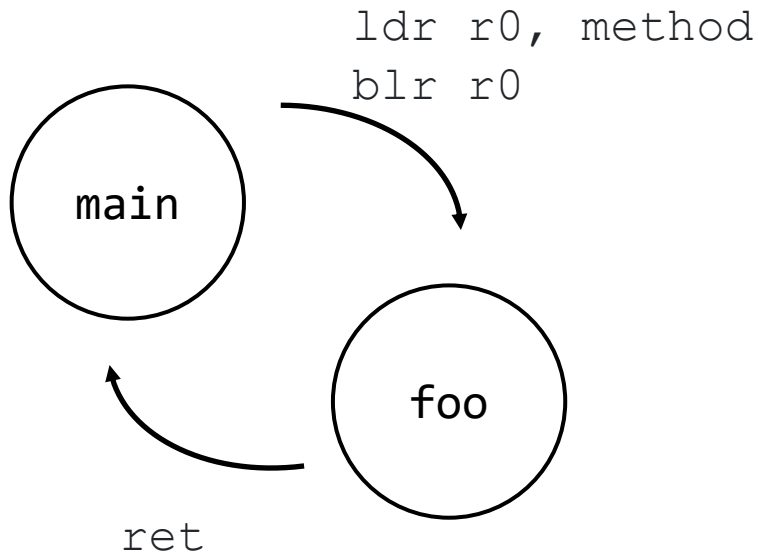


INTRODUCTION

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```
void foo() { ... }  
  
void main() {  
    ...  
    obj->method = foo;  
    obj->method();  
    ...  
}
```

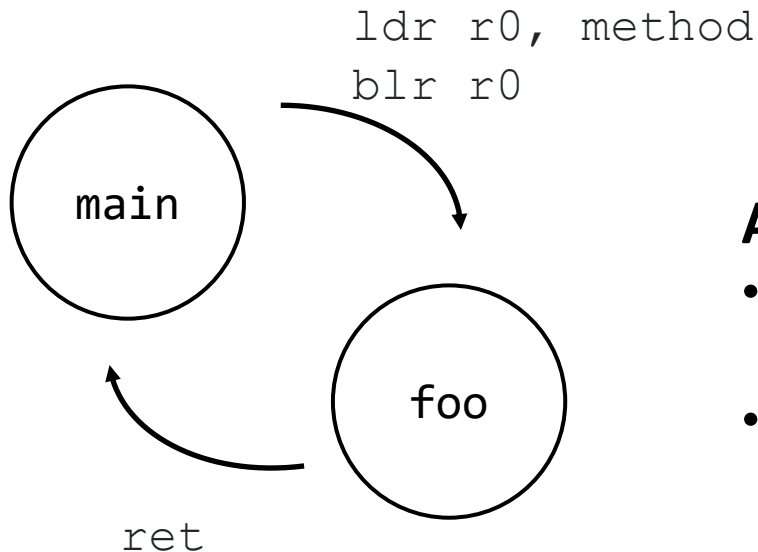


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ARM introduced hw supports:

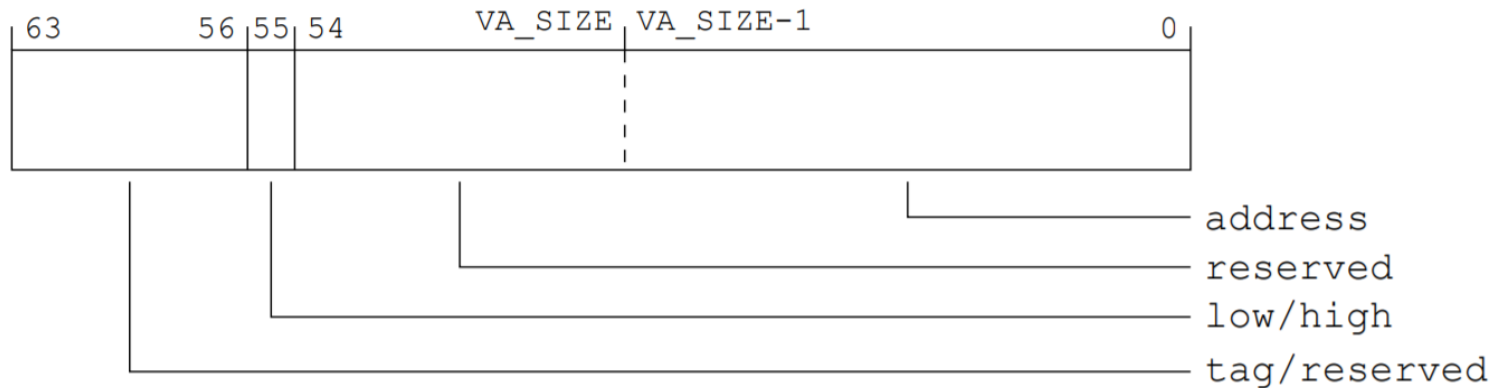
- Branch Targets Identification (**BTI**)
 - Forward branch protection
- Pointer Authentication Code (**PAC**)
 - Backward branch protection



BACKGROUND

Pointers in AArch64:

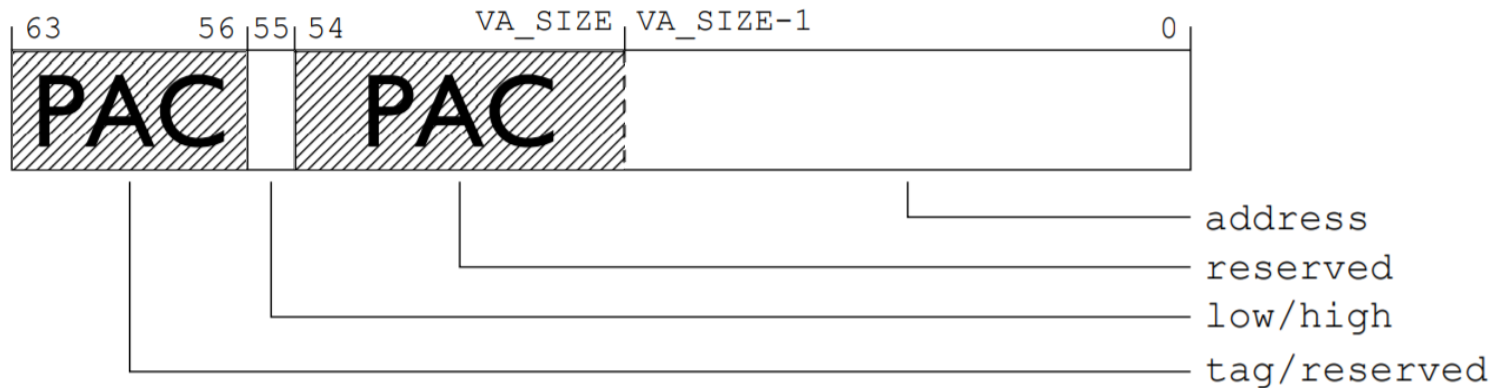
- Address represented on $[0:VA_SIZE]$
- Typically $VA_SIZE = 48$
- Empty $[VA_SIZE:54]$ and $[56:63]$



BACKGROUND

AArch64 Pointer Authentication Codes (PAC):

- Hardware-based CFI
- Leverages empty space on 64-bit virtual addresses
- Append a Message Authentication Code (MAC)



BACKGROUND

Introduced two insns:

- PAC
- AUTH

PAC Creation takes:

- A pointer
- A 64-bit context
- A 128-bit secret key

PAC algorithm 'H' can be:

- QARMA
- Implementation defined



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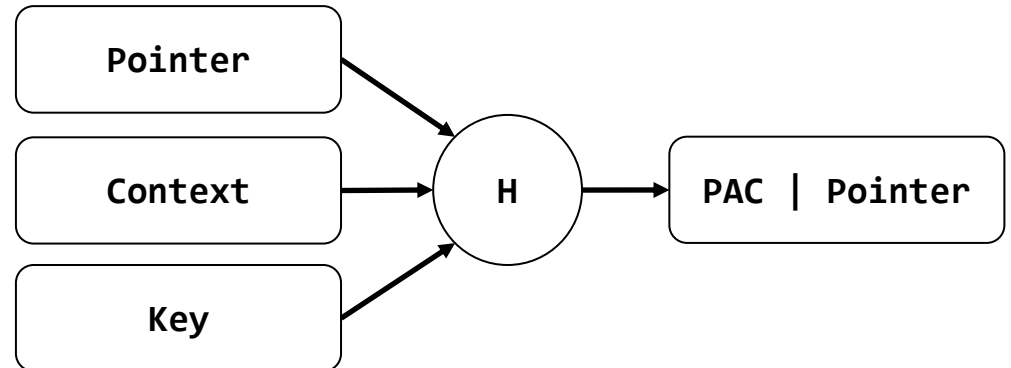
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PAC:



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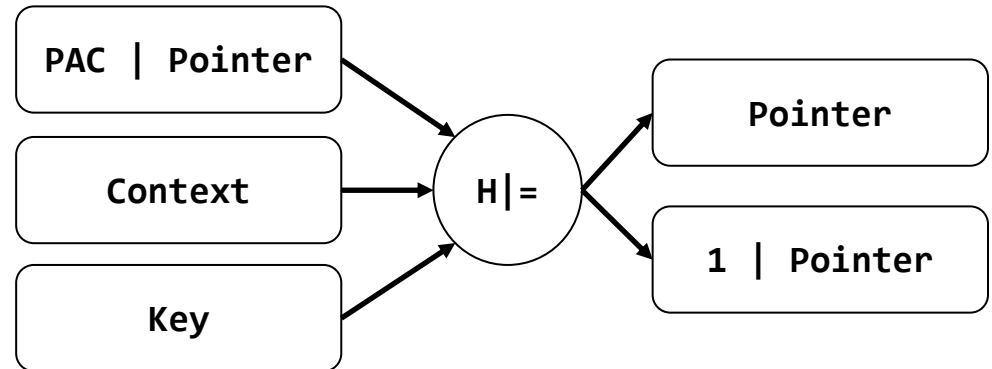
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Pointer authentication ISSUES

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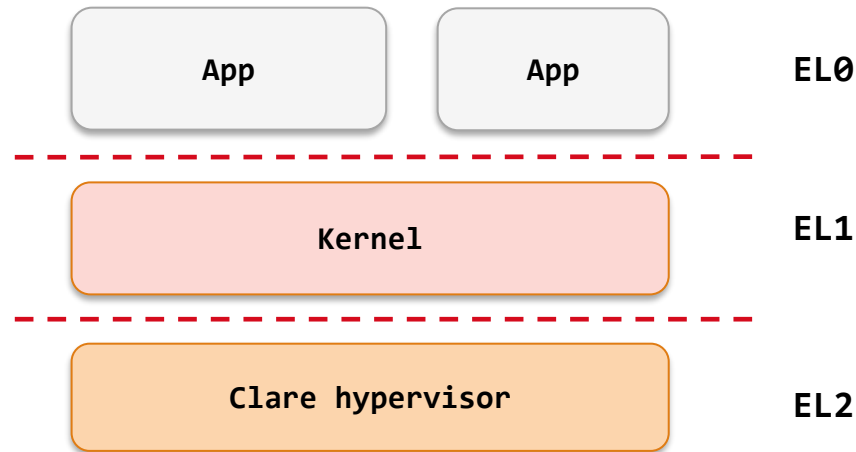
**Leverage on
virtualization to
counteract these
issues!**



PROPOSED APPROACH

Leverage on CLARE hypervisor to:

1. Improve key management
2. Provide PA to all AArch64 SoC

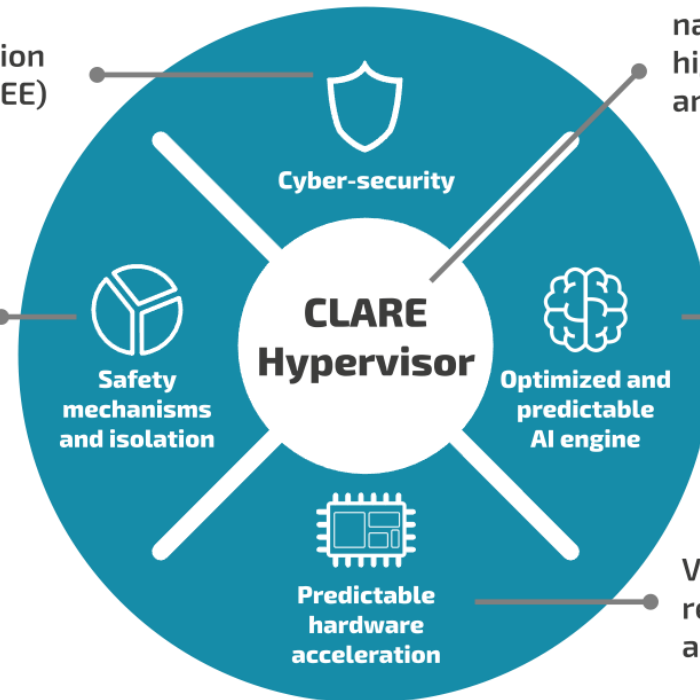


CLARE IN A NUTSHELL

clare

Multi-stage Secure Boot
Address-space layout randomization
Trusted Execution Environment (TEE)
Control-flow Integrity

Health monitoring, temporal
and spatial isolation for mixed-
criticality applications



Minimal, bare-metal type-1 hypervisor
natively designed for being secure, safe,
highly-configurable, portable,
and suitable for SIL3/4 certification

Optimized execution framework
for machine learning algorithms
that guarantees safety (via run-
time monitoring) and predictability

Virtualization of hardware acceleration
resources with predictable behavior
and isolated execution



AUTOMOTIVE



AEROSPACE



DRONES



RAILWAYS



MANUFACTURING 4.0

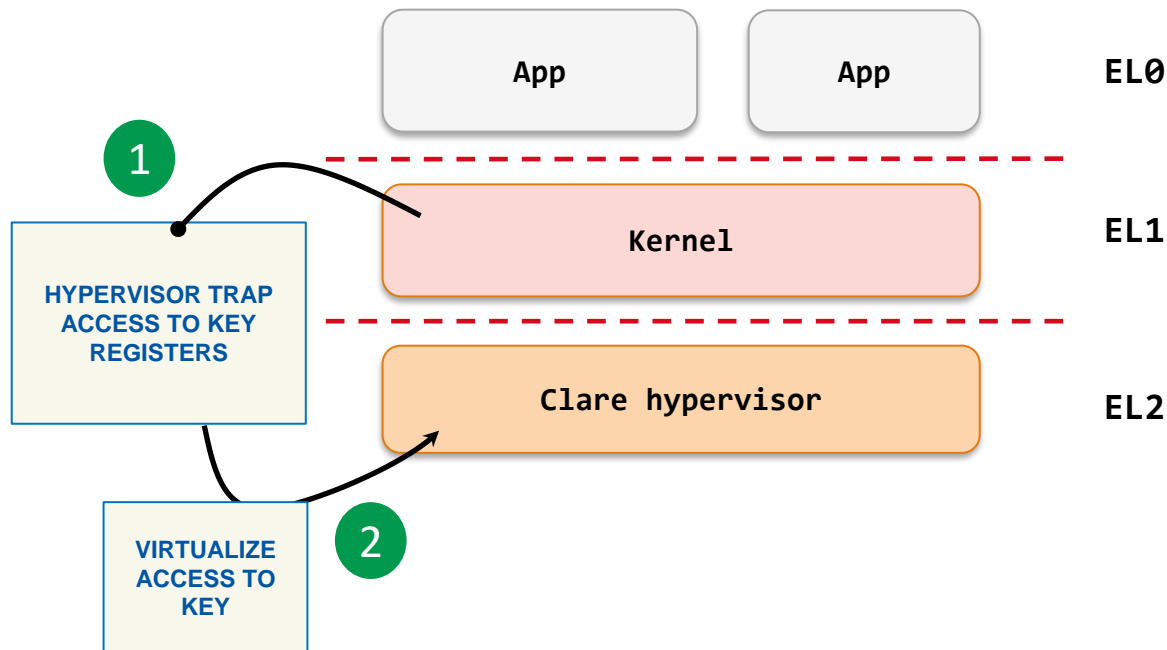


Check it out @ clare.santannapisa.it

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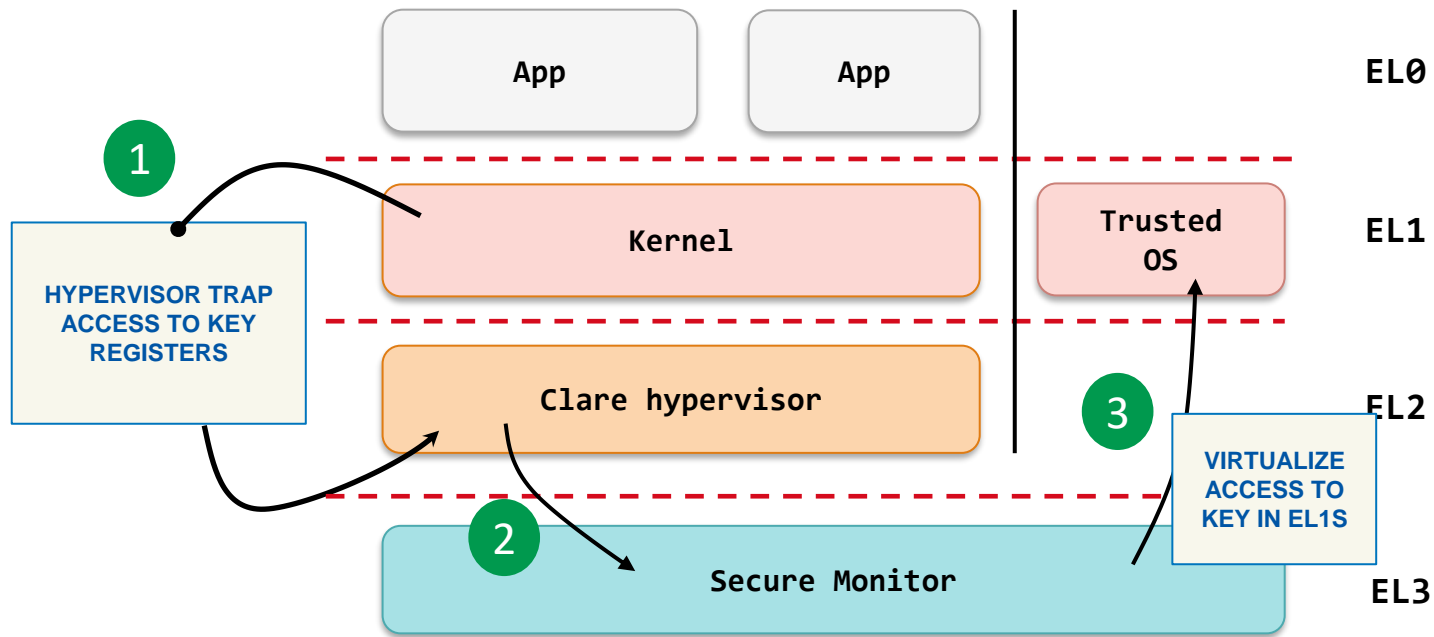
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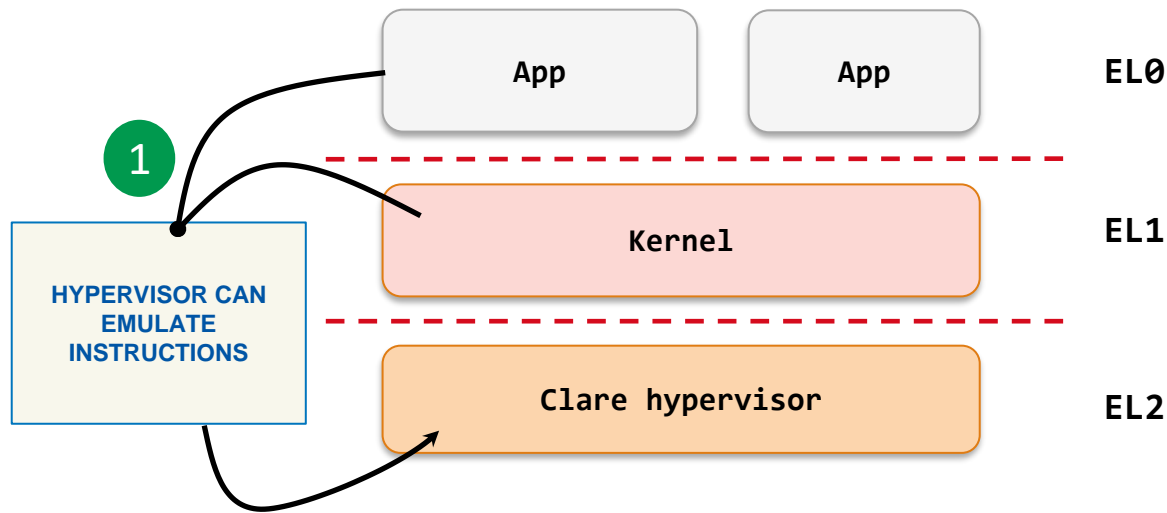
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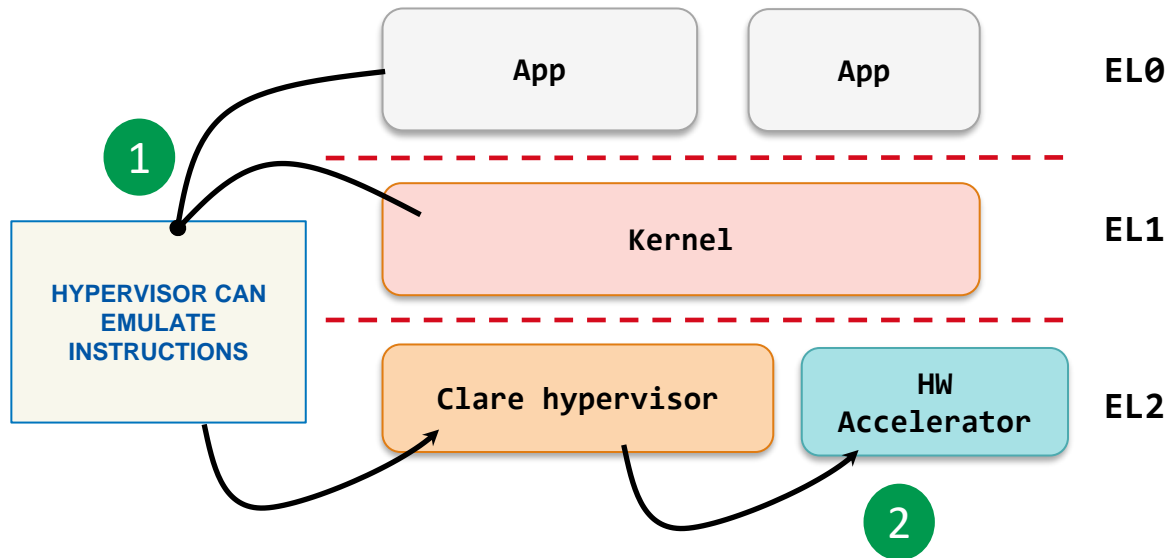
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2. Provide PA to all AArch64 SoC
 1. PA can be HW accelerated
 2. **Clare** can detect attacks



CONCLUSIONS & FUTURE WORKS

Advances in embedded system connectivity and technologies need to be followed by corresponding advancements in associated security protection!

Future directions

- Measure aggregate overhead when protecting 1 domain out of N
- Apply PAC in selective way (only “more at risk” processes)
- Simplify access to PAC features
- Fully integrate the stack for production in **CLARE** hypervisor



THANK YOU

QUESTIONS?

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